SINGLE EVENT EFFECTS AND RADIATION HARDENING METHODOLOGIES IN SIGE HBTS FOR EXTREME ENVIRONMENT APPLICATIONS

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Stanley D. Phillips

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SINGLE EVENT EFFECTS AND RADIATION HARDENING METHODOLOGIES IN SIGE HBTS FOR EXTREME ENVIRONMENT APPLICATIONS

Approved by:

Professor John D. Cressler, Advisor
School of Electrical and Computer Engineering
Georgia Institute of Technology

Professor John Papapolymerou
School of Electrical and Computer Engineering
Georgia Institute of Technology

Professor A. P. Meliopoulus
School of Electrical and Computer Engineering
Georgia Institute of Technology

Professor Oliver Brand
School of Electrical and Computer Engineering
Georgia Institute of Technology

Professor Walter de Heer
School of Physics
Georgia Institute of Technology

Date Approved: October 8, 2012

For my mother and father,

who challenged me to be the best in myself.

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SUMMARY

Field-effect transistor technologies have been critical building blocks for satellite systems since their introduction into the microelectronics industry. The extremely high cost of launching payloads into orbit necessitates systems to have small form factor, ultra low-power consumption, and reliable lifetime operation, while satisfying the performance requirements of a given application. Silicon-based complementary metal-oxide-semiconductors (Si CMOS) have traditionally been able to adequately meet these demands when coupled with radiation hardening techniques that have been developed over years of invested research. However, as customer demands increase, pushing the limits of system throughput, noise, and speed, alternative technologies must be employed. Silicon-germanium BiCMOS platforms have been identified as a technology candidate for meeting the performance criteria of these pioneering satellite systems and deep space applications, contingent on their ability to be hardened to radiation-induced damage. Given that SiGe technology is a relative new-comer to terrestrial and extra-terrestrial applications in radiation-rich environments, the same wealth of knowledge of time-tested radiation hardening methodologies has not been established as it has for Si CMOS. Although SiGe BiCMOS technology has been experimentally proven to be inherently tolerant to total-ionizing dose damage mechanism, the single event susceptibility of this technology remains a primary concern. The objective of this research is to characterize the physical mechanisms that drive the origination of ion-induced transient terminal currents in SiGe HBTs that subsequently lead to a wide range of possible single event phenomena. Building upon this learning, a variety of device-level hardening methodologies are explored and tested for efficacy in the context of device and circuit implementations.

CHAPTER I

INTRODUCTION

The advent of the integrated circuit (IC) has spurred a technological revolution which has reshaped countless aspects of the lives of individuals across the globe. As technology scaling on both bipolar and field-effect transistors has matured from discrete components to very large scale integration (VLSI) on a single semiconductor wafer, the possibility for system on a chip (SoC) solutions has emerged. SoC applications have fueled the markets for analog/mixed signal, radio frequency, mm-wave, and wired/wireless high speed communications applications. A bounty of semiconductor technologies have emerged as contenders for employment in these applications (including but not limited to III-V, silicon-on-sapphire, silicon-on-insulator, radio-frequency CMOS, and silicon-germanium) each boasting their own characteristic strengths and weaknesses. As system specifications become increasingly stringent, the need for improved device metrics that match the requirements of a specific application becomes increasingly important. This is essential for niche markets that have highly specific needs and generally operate in unique environmental conditions. One such niche market, which is becoming increasingly important (and challenging), is extreme environments.

Extreme environments encompass the operation of electronic systems in surroundings which exist outside of the domain of standard commercial or military specifications [17]. These environments can include any combination of extreme high/low temperatures, large amounts of mechanical stress, chemical corrosion, or intense radiation fields. One market that encounters many of these environmental extremes is space-borne electronic systems. Space is a very diverse, hostile environment whose surroundings vary

upon the type of application being pursued. Temperatures can vary from cryogenic (deep-space probes) to extremely high (illuminated lunar craters) and radiation levels are highly dependent on the altitude from the earth's surface. Any technology to be used in these applications must be tolerant to both temperature and radiation-induced effects. Silicon-germanium technology has arisen as suitable platform for incorporation in space-based electronic systems given its high speed, low cost, compatibility with silicon CMOS technology, and intrinsic excellent low temperature performance. The radiation response of silicon-germanium devices (specifically the occurrence of single event effects) and methods to harden this technology to these degrading effects is still an on-going area of research.

Radioactive particles in space originate from numerous sources including particles ejected from the corona of the sun (solar winds), charged particles trapped in the magnetic fields of large solar bodies, and background galactic cosmic rays (a cosmic stew of extremely high energy ions, protons, and photons) [95]. The Van Allen belts, consisting of energetic protons and electrons that have become trapped by the earth's internal magnetic field, are of particular concern for orbital applications [59]. Any electronic system which operates while being exposed to these sources is liable to suffer from a broad range of detrimental effects. These effects include displacement damage of the bulk semiconductor material, ionization damage in the oxides of the semiconductor and oxide-semiconductor interfaces, and a compendium of single event effects (SEEs). As semiconductor technologies continue to mature with increased device scaling, radiation susceptibility becomes a growing concern for reliable operation of electronics in space environments.

Silicon-germanium heterojunction bipolar transistors (SiGe HBTs) have been repeatedly shown to be inherently resilient to total ionizing dose and displacement damage [99, 97, 6, 57], while significant vulnerability to SEEs has been identified [87, 49, 48, 96]. To address this sensitivity, radiation hardening mechanisms employed on

both the device and circuit-architecture level are being investigated. The most common hardening methodologies encountered are radiation hardening by process (RHBP), which entails modifications to fabrication steps (additional masks), and radiation hardening by design (RHBD), which involves alterations to circuit architectures or changes to device structure (does not interrupt normal fabrication flow). Given that RHBP can be extremely costly and forces a foundry to break away from their process of record, it is highly desirable to pursue RHBD techniques that achieve acceptable levels of radiation tolerance while maintaining low system costs.

1.1 SiGe BiCMOS Technology

The concept of incorporating germanium into a silicon material system is far from new and was first conceptualized by William Shockley in the days of the primitive transistor. Despite its early origins, the reality of silicon-germanium (SiGe) alloys would not manifest until several decades later, once processing technology evolved to allow device-suitable SiGe films to be manufactured. Today, ultra-high vacuum chemical vapor deposition (UHV/CVD) and molecular beam epitaxy (MBE) provide the process techniques necessary to grow extremely thin, defect-free SiGe films. Given the lattice mismatch between a SiGe alloy (exact value dependent on the germanium fraction following Vegard's rule [19]) and a Si substrate, SiGe films will experience biaxial compressive strain to adopt the same crystalline structure as the underlying silicon material. If the film thicknesses exceeds a specified value (termed critical thickness, calculated from several variables including total germanium content and buffer layer thicknesses), films will relax forming misfit dislocations as illustrated in Figure 1. These dislocations are unsuitable for transistor operation, generating substantial leakage paths for current. Replacing the base region of a standard silicon bipolar transistor with a thin epitaxially-grown SiGe film essentially forms the SiGe heterojunction bipolar transistor (SiGe HBT). This device can be integrated with standard CMOS

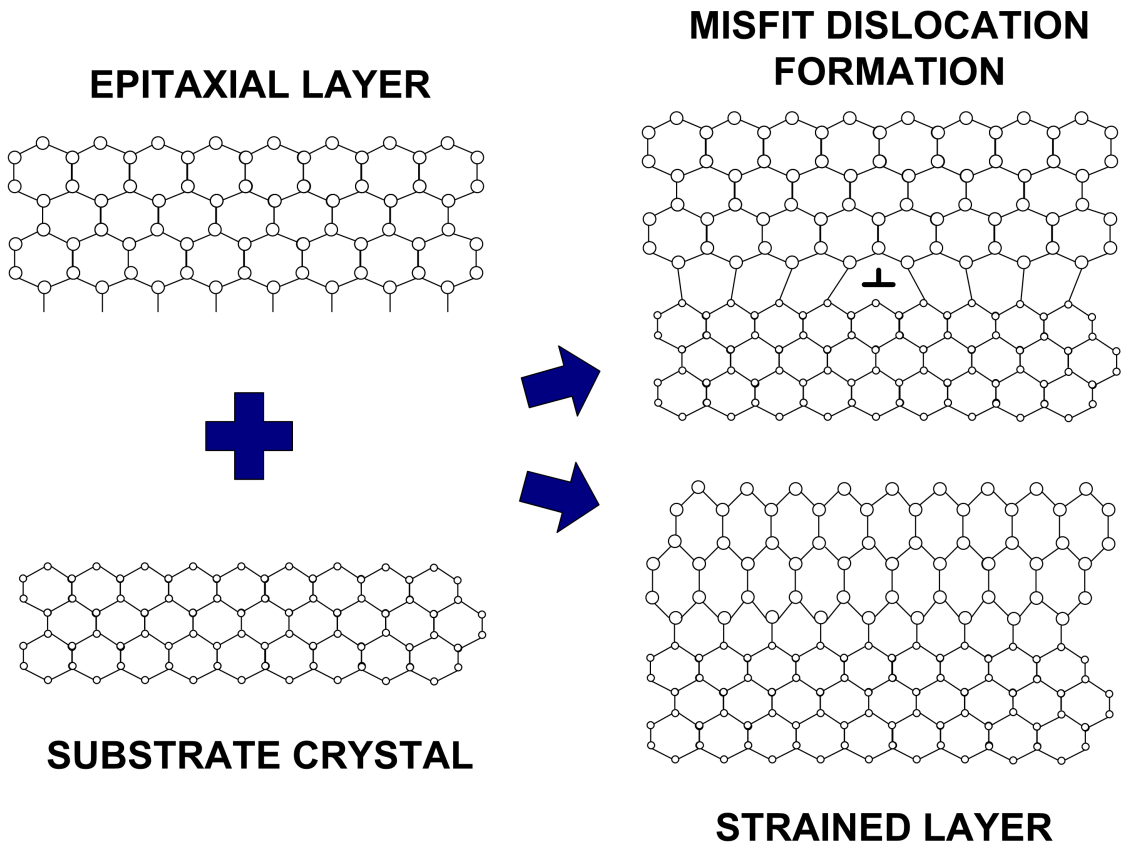


Figure 1: A conceptual representation of two possible outcomes for lattice mismatched epitaxial growth: a strained layer or a relaxed layer with misfit dislocations. (After [8])

fabrication (with minimal increase to mask layers) to form a hybrid SiGe BiCMOS platform that allows IC designers to take advantage of both high-performance bipolar and highly-integrated silicon CMOS.

The growth and inclusion of a SiGe film in a silicon transistor represents the first successful attempt at bandgap engineering in a silicon system. When comparing silicon and germanium as bulk materials it is evident that germanium has many material properties superior to that of pure silicon, as shown in Table 1. Intuitively, it is expected that mixing these two elements will result in an alloy whose material properties are more desirable than pure silicon. Through the inclusion of germanium in a silicon system, devices can be tailored to improve their performance by adjusting

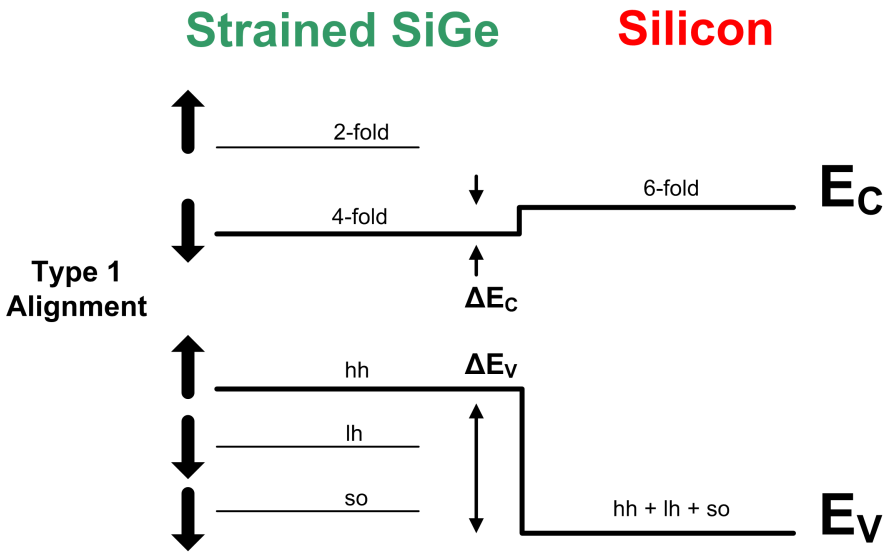


Figure 2: Band alignments of a strained SiGe alloy grown on a silicon wafer. The break in band degeneracies as well as the offsets in band edges is highlighted. (After [19])

a variety of operational characteristics. Given that germanium has an intrinsically smaller bandgap than silicon, a SiGe film will also have a smaller bandgap. By replacing the base of a standard silicon bipolar transistor with a strained SiGe alloy (physically consisting of a SiGe alloy sandwiched between two intrinsic silicon layers), a type-I energy band alignment is obtained. The band edges of the SiGe material are contained with the silicon band edges, as illustrated in Figure 2.

As seen in the figure, the dominating offset is the discontinuity in the valence bands (E_V), which is highly desirable. Additional effects induced by the compressively

Table 1: Device-relevant material parameters for both bulk silicon and germanium (After [84]).

Parameter	Silicon	Germanium	Units
E_g	1.12	0.66	eV
m_n^*/m_o	1.18	0.55	–
m_p^*/m_o	0.81	0.36	–
μ_n	1350	3900	$cm^2/V\times$s
μ_p	480	1900	$cm^2/V\times$s
a	5.43	5.66	Å

strained SiGe layer include a break in the band degeneracies, an increase in majority-carrier hole mobility (for p-type material), a decrease in minority carrier electron mobility (p-type material), and a decrease in the density of carrier states (N_C and N_V).

An additional tuning knob for optimization of device-performance metrics of SiGe HBTs at an engineer's disposal is the grading profile of germanium. Grading germanium in the base of an HBT will result in a graded bandgap throughout the base, which will manifest itself in the conduction band of the energy band diagram of the HBT. The translation from an initial valence band offset to a conduction band offset in the complete energy band diagram can be understood through the following discussion. The acceptor doping in the base is constant; therefore, the Fermi level and the difference between the Fermi level and valence band are fixed. The transistor is also in a state of equilibrium, forcing the Fermi level to be constant. To accommodate these conditions while maintaining the reduction in badgap with graded germanium, the conduction band is forced to change. An energy band diagram for a graded germanium SiGe HBT operating in forward active mode is shown in Figure 3.

In addition to the normal band bending present in forward-active mode, an additional bend in the conduction band is present in the neutral base region. This bending is a result of the germanium grading effect discussed previously. Recalling the interrelationship between band-bending and electric fields as described by Equation 1, it is evident that an additional drift field will be present in the base, boosting device performance.

$$\varepsilon = -\frac{dV}{dx} = \frac{d(\frac{-(E(x)-E_{ref}(x))}{q})}{dx} \tag{1}$$

This inherent drift field will accelerate minority carrier electrons across the base, reducing the base transit time (classically the metric dominating maximum operating

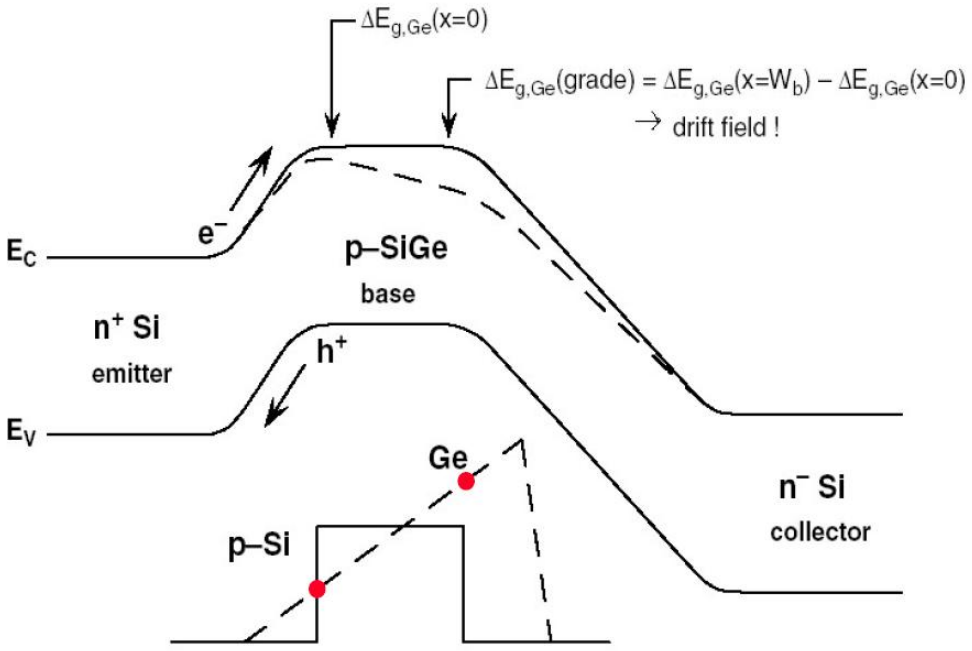


Figure 3: Energy band diagram of an NPN SiGe HBT operating in forward-active mode Germanium-induced effects are highlighted on the energy band diagram (After [19]).

frequencies of devices). The band offset at the emitter-base junction will also provide a performance enhancement, boosting the collector current of the device while maintaining the same base current, increasing device gain. For a full discussion of the impact and benefits of a graded germanium base profile on device physics, the reader is directed to [18].

1.2 The Space Environment

The serene night sky seen from the surface of the earth is misleading in terms of the actual environment that exists in space. Above the earth's protective atmosphere the sky is reeling with highly energetic particles that are extremely harmful for both humans and electronic systems. To complicate matters further, the radiation environment of space is also incredibly dynamic. The exact environment encountered for an application on a given space mission is dependent on numerous variables

including the current solar cycle, the orbital path and altitude of a craft, and the duration of the orbit. The possible earth orbits can be broken down into four categories low earth orbit (LEO, below an altitude of 10,000 km), medium earth orbit (MEO, between 10,000 to 20,000 km), geostationary orbit (GEO, at 36,000 km), and highly elliptical orbit (HEO) [60]. Each orbit is subject to various particle sources, types, and intensities. To guarantee that our satellites and other spacecraft are operational in this extremely harsh environment, a detailed understanding of the various sources of space radiation and their interactions with microelectronic systems is necessary.

The Van Allen radiation belts arise from the magnetosphere of the earth, which traps charged particles ejected from the sun (solar winds) forming a plasma torus around the earth, as seen in Figure 4. These belts are composed of trapped electrons, protons, and low-energy heavy-ions that gyrate and traverse along magnetic field lines.

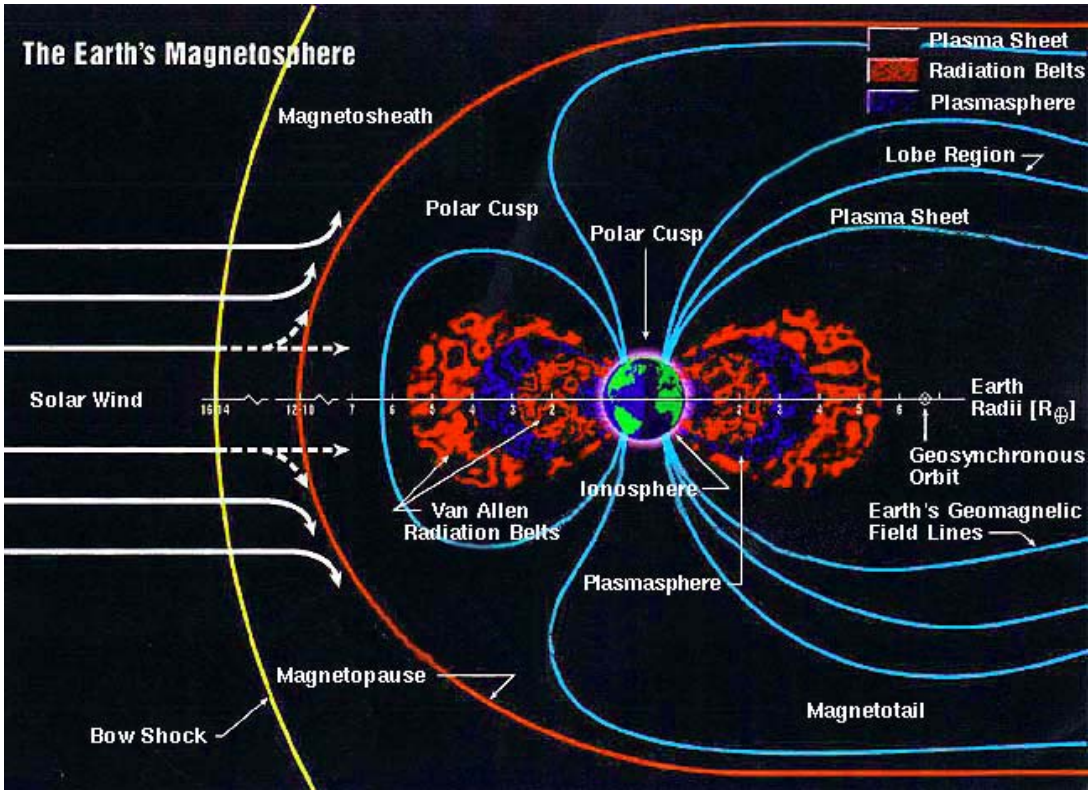


Figure 4: Van Allen belts surrounding the earth, fueled by solar winds and held in place by the earth's magnetic field (After [71]).

Trapped electrons and protons, which can have very large energies (the low-energy heavy ions can be blocked with minimal shielding), are the primary concern for orbital electronics. The electrons in the Van Allen belts can be broken into two zones, an inner zone and an outer zone. The inner zone extends outwards to about two and four tenths earth radii, and is composed of a spectra of lower energy electrons (<five MeV); meanwhile, the outer zone (beginning at two and eight tenths earth radii and stretching out to twelve earth radii) has an energy spectra that extends up to seven MeV [95]. Unlike electrons trapped proton distributions can not be broken into zones, given that their spatial coordinates vary inversely with their energy as seen in Figure 5. Proton energies can extend from several hundred MeV close to the earth's atmosphere to a few MeV on the outer edges of the Van Allen belts. The relative fluxes of the particles in these belts are strongly dependent on the current solar cycle and satellite altitude.

A troublesome characteristic of the Van Allen radiation belts is the presence of the

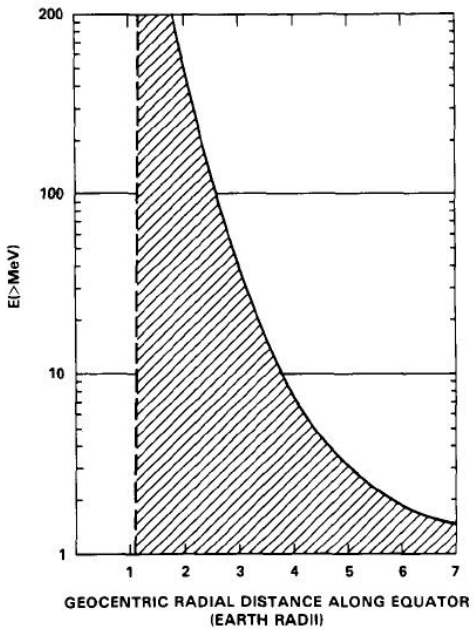


Figure 5: Energy of trapped protons as a function of distance from the earth's surface (After [95]).

South Atlantic Anomaly (SAA) [60]. The SAA is a depression in the earth's magnetic field over the north eastern coast of South America. Trapped particles contained within the SAA are the closest to the earth's atmosphere than any other particle in the Van Allen belts. These particles (particularly the very high energy protons which are characteristically close to the earth's atmosphere) are of particular concern for LEO applications that pass through this region of space [95]. The SAA is another demonstration of the importance of understanding every aspect of an orbital mission before a prediction of the total radiation environment encountered can be made.

The other spectrum of radioactive particles in space includes un-trapped radiation. This radiation originates from ejected particles from the sun's corona (solar flares) and

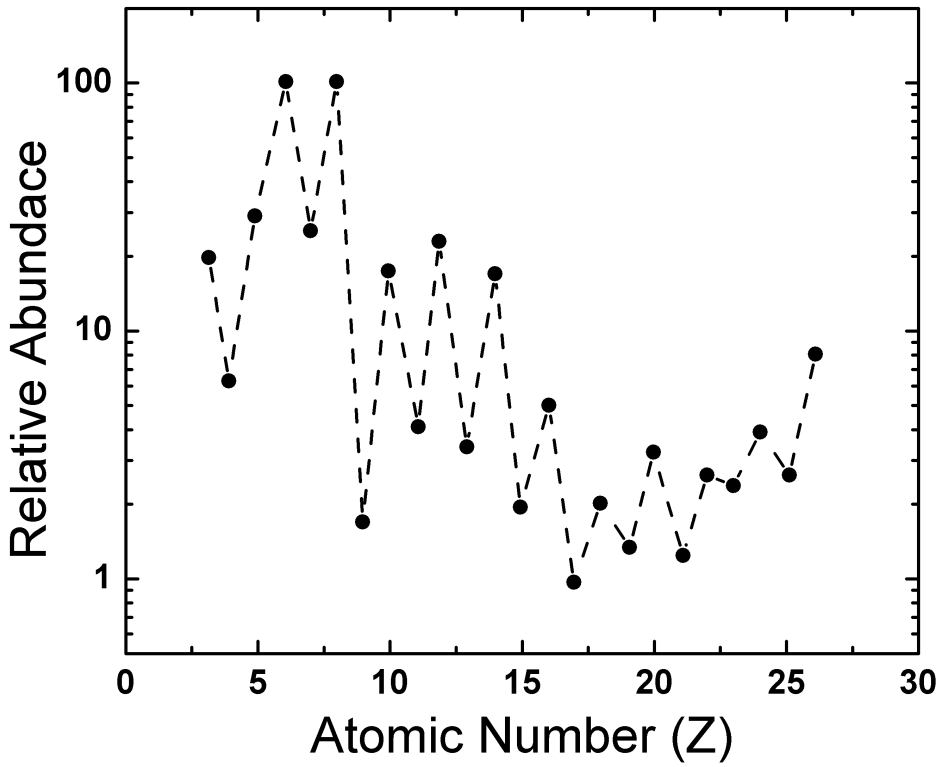


Figure 6: Relative distribution of elements contained in galactic cosmic rays (After [95]).

galactic cosmic rays [95]. Both radiation sources are primarily composed of high energy protons, high energy protons, and photons. Solar flares are a periodic occurrence that correspond to the solar cycle (peaking at a solar maximum); however, galactic cosmic rays are an ever present threat to electronic systems operating in GEO, HEO, or deep space (systems operating in LEO to MEO are generally shielded from these highly energetic transiting particles by the geomagnetic field of the earth). The source of galactic cosmic rays is a disputed topic, but is believed to be remnants of supernova explosions [66]. Despite controversy over their origins, the compositions and energy spectra of galactic cosmic rays are well understood (which is of utmost importance to a radiation effects engineer!). The relative distribution of elements in galactic cosmic rays based on their atomic charge is shown in Figure 6. These particles typically have energies which peak around one GeV/nucleon when they are near the earth. Given their high energies, these particles are deeply penetrating, and sensitive electronics can not be effectively shielded using aluminum plating with reasonable thicknesses.

1.3 Radiation Effects in SiGe BiCMOS Technology

Having established the details of the various radiation components in a space environment, it is logical to move into a discussion of the impact of these sources on microelectronic systems operating in these environments. Although the focus will be on radiation effects in a SiGe bipolar system, the importance of understanding the effects on all system components should not be disregarded. The effects of radiation on SiGe HBTs can be classified in the following three catergories ionization damage (total ionizing dose, TID), displacement damage (DD), and single event effects (SEEs). Comprehensive research has been performed over the decades to understanding and minimizing the detrimental effects associated with TID and DD across a multitude of semiconductor platforms and generations. SiGe technology has been repeatedly shown to be resilient to TID damage, maintaining nominal device operation with minimal

degradation at typical bias values [6, 97, 99, 57]. However, SiGe technology has also been shown to be quite vulnerable to single event effects [87, 69]. In the following sections the specifics of TID/DD and SEE are presented. Single event upset (SEU) is identified as a particular concern in the realm of SEEs, and the physical origin of this effect is discussed.

1.3.1 Total Ionizing Dose & Displacement Damage

As an energetic ionizing particle (photon, electron, proton, heavy ion, etc.) passes through a semiconducting/insulating material, it will deposit energy in the system resulting in the ionization of electron/hole pairs. The total amount of energy absorbed by a material is defined as the rad (radiation absorbed dose), a material-dependent quantity, and is used to quantify the total ionizing dose received by a material. The rad is defined as 100 ergs per gram of energy absorbed by a given material and is calculated through Equation 2

$$rad = LET \times fluence \times 1.60 \times 10^{-5}, \tag{2}$$

where the LET is a material-dependent variable that quantizes the rate of energy loss of the particle and fluence is the total number of particles striking a material [60]. Depending on the particle type, energy loss is accomplished through various means including but not limited to elastic scattering (electrons, protons, and heavy ions), photoelectric effect (photons), and pair production (photons) [16]. In the bulk of a semiconductor material, this ionized charge does not have long-term detrimental effects; however, insulating materials (specifically oxides in a semiconductor system) are susceptible to being damaged by this charge. If a particle has sufficient mass and momentum, it can experience an in-elastic scattering event in the silicon lattice, where an atom from the semiconductor lattice is physically displaced. This process is termed displacement damage, and occurs for proton, neutron, and heavy-ion radiation. The traps formed from these vacancies are dispersed throughout the energy bandgap

of the semiconductor and can have a range of effects on the device. These effects include increases in resistances from dopant deactivation, reductions in carrier mobility from increased scattering events, increases in leakage currents from thermal carrier generation, and increases in carrier tunneling across barrier due to reductions in potential height and widths [19]. As technologies mature and scale in size, the volumes of transistor active regions shrink, decreasing the effects of displacement damage on a device.

Holes that are created in an oxide material due to ionizing radiation exposure are the primary damaging mechanism for semiconductor. These holes either become trapped within the oxide, forming fixed charges in the oxide bulk, or migrate to oxide-semiconductor interfaces due to electric field lines in the oxide. At the interfaces, holes can interact with dangling oxygen bonds that are passivated with hydrogen, breaking these bonds and forming interface charge traps [73]. These trapped charges and interface states will lead to increases in device leakage (correlating to gain degradation in a bipolar technology). The sensitive oxides for SiGe HBTs include the emitter-base spacer oxide and the shallow trench isolation (STI) oxide, as demonstrated in Figure 7.

Given that the emitter-base and base-collector depletion regions overlap these oxides, any traps at the oxide-semiconductor interface (D_{it}) will increase the amount of surface recombination, adding to the base leakage currents and reducing gain. Numerous TID studies have been performed on multiple generations of IBM's SiGe BiCMOS technology. In addition to varying technology generations, these studies also looked at the impact of different radiation sources, dose rates, and temperatures [97, 99]. Overall SiGe BiCMOS technology is found to be resilient to total dose damage that generates base leakage currents primarily in low-injection regimes (where devices in circuits are rarely biased). As an example, a representative post 63 MeV proton irradiation gummel plot of a third generation SiGe HBT is shown for various total

dose values in Figure 8. A gradual rise in base leakage current is evident as the total absorbed dose increases, indicative of an increase in trap density within the sensitive emitter-base spacer oxide. This leakage is present only in the low-injection regime (base bias values <800mV) and quickly falls below the background forward-diffusion current for bias voltages above this regime. The robust nature of SiGe HBTs to TID can be attributed to several features of the technology including their minimal overlap of oxides over sensitive device regions, heavy doping of the extrinsic base, and an oxide/nitride composite composition. As SiGe technology continues to scale and mature, tolerance to both DD and TID will improve, as active volumes and oxides shrink in size.

1.3.2 Single Event Effects

While TID and DD describe accumulated damage to a semiconductor system, SEEs describe transient effects which can either have short or long term consequences. Single event effects encompass a broad range of deleterious errors, which range from

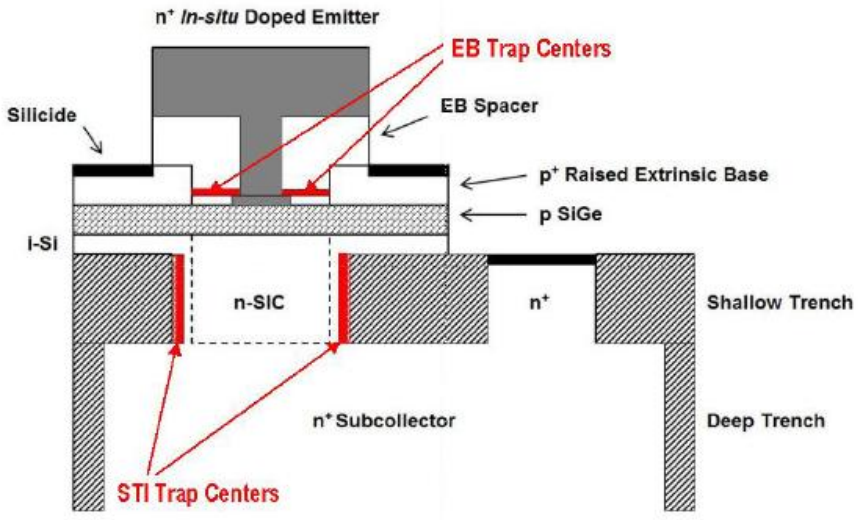


Figure 7: Cross section of 3^{rd} generation SiGe platform with sensitive oxides clearly illustrated (After [19]).

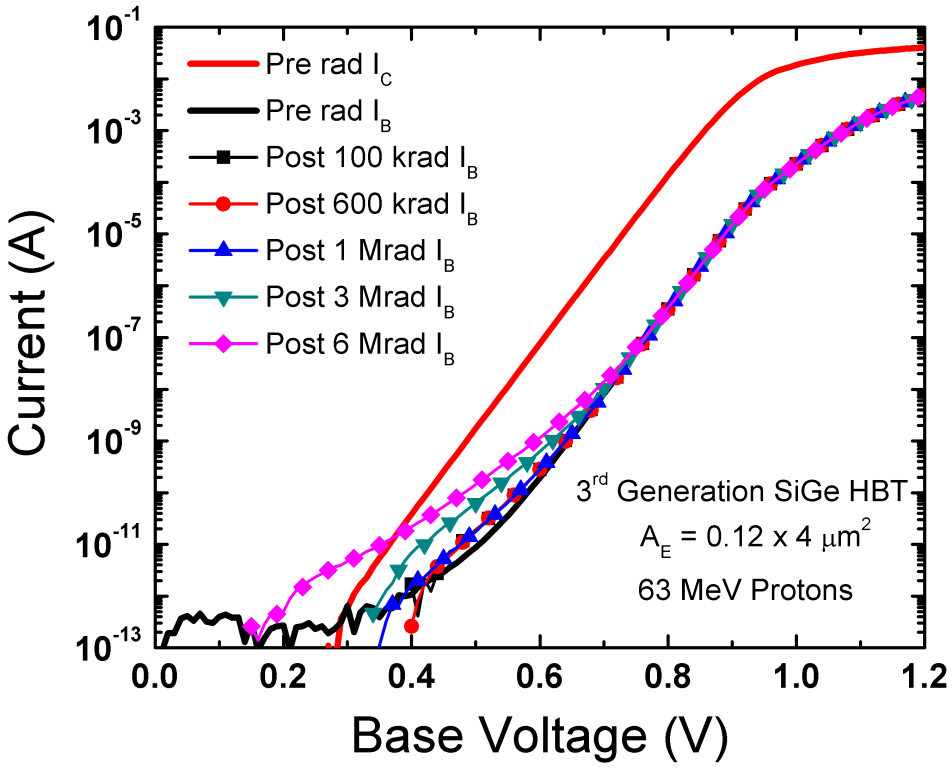


Figure 8: Characteristic TID degradation of the low-injection base current resulting from 63 MeV proton exposure.

destructive or hard errors to recoverable or soft errors. Despite the wide range of SEEs that exist, each type of error originates from the same phenomena; a highly concentrated track of charge pairs generated in the bulk of a device which interact with surrounding depletion regions and electric fields as the free carrier concentration is restored to equilibrium levels. A summary of the different types of errors is provided in Table 2. Orbital satellite communications ubiquitously encompass high-speed digital logic blocks; therefore, the upset of a digital logic state (SEU/MBU) is a foremost concern for satellite system designers. Sensitivities to SEU have been shown to increase as system clocking speeds have increased [14], further motivating the need to understand and mitigate these errors.

As an energetic charged particle passes through a semiconductor material it deposits energy in the form of ionized charge (electron-hole pairs) along its trajectory, forming a dense track of mobile charge pairs. A metric for describing the amount of energy

lost by a particle through a material (and a means for calculating the total charge generated) is the linear energy transfer (LET). The LET of a particle defines the energy loss per unit path length, normalized by the density of the material. The most standard units of LET are $\frac{MeVcm^2}{mg}$. The value of a particle's LET depends on a wide range of parameters including the particle mass, particle energy, and target material. With the LET the total amount of charge deposited can be calculated, since the energy required to generate a single electron-hole pair is known for a given material target. The density of electron-hole pairs that are generated within the charge track is typically between 10^{18} and 10^{19} cm^{-3}; several orders of magnitude higher than the background doping of the substrate of standard semiconductor technologies [61]. For just a bulk piece of semiconductor material, this charge will diffuse radially outward, through the process of ambipolar diffusion (to maintain neutrality of the charge plasma), until enough recombination events have taken place to restore the free carrier concentration to equilibrium levels. For an IC, which contains devices composed of p-n junctions, there are several different mechanisms which take place aside from ambipolar diffusion to reestablish equilibrium conditions of free carrier concentrations. These other mechanisms can have detrimental affects on the operation of a circuit containing a device which has been struck with an energetic charged particle.

If a particle passes directly through the depletion region of a p-n junction, the

Table 2: Compendium of Single Event Effects.

Acronymn	Effect	Error Type	Sensitive Technologies
SEL	Single Event Latch-up	Hard	Primarily FETs
SEGR	Single Event Gate Rupture	Hard	FETs
SEB	Single Event Burnout	Hard	JFETs, Diodes
SET	Single Event Transient	Soft	HBTs, FETs
SEU	Single Event Upset	Soft	HBTs, FETs
MBU	Multiple Bit Upset	Soft	HBTs, FETs
SEFI	Single Event Functional Interrupt	Hard	FETs, HBTs

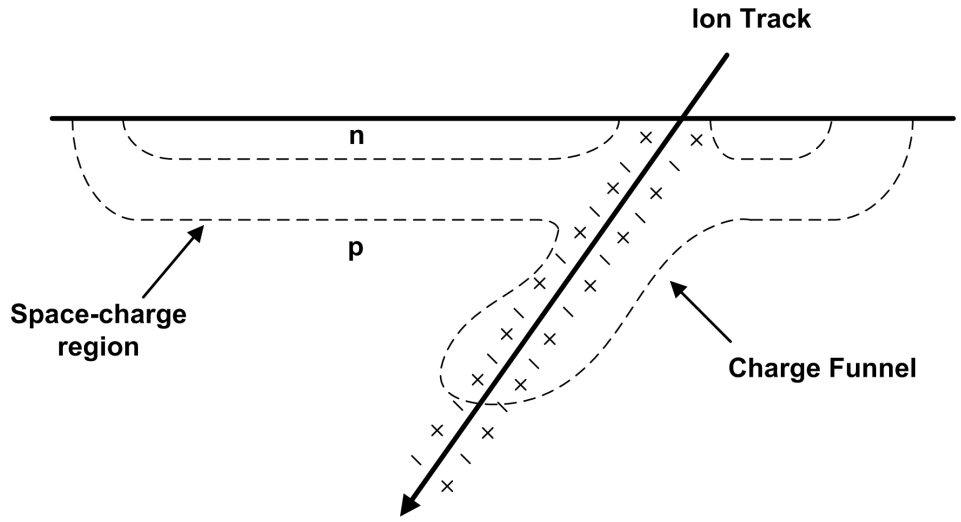


Figure 9: Generation of a modulation in the substrate potential and depletion region of a struck junction, resulting in the funneling effect (After [19]).

deposited charge will result in several different phenomena occurring. First, the electric field lines of the depletion will result in the separation of electron-hole pairs, with electrons drifting towards the n-type material and holes drifting towards the p-type material. Second, given the large densities of mobile charge carriers generated by a particle, these charges will screen the electric field lines contained within the depletion region. As a result the depletion region will collapse and the electric field lines, which were initially confined within the depletion region, are pushed outwards to maintain the applied voltage across the junction. This distortion of the electric field lines is classically known as the funnel effect [61, 26, 27] and is illustrated in Figure 9. With electric fields stretching deeper into the substrate, a greater amount of deposited charge is collected (a more accurate description is to say charge is induced on terminals) by the contacts on the n-type and p-type materials. The funneling effect is not limited to only instances where the particle passes directly through a depletion region. Substrate doping is relatively low for most commercial semiconductor technologies ($\approx 10^{14}$ - 10^{15} cm^{-3}); therefore, the diffusion length of carriers can be relatively large ($\approx$100 μm in a silicon system with substrate doping in this range). As a result, significant charge

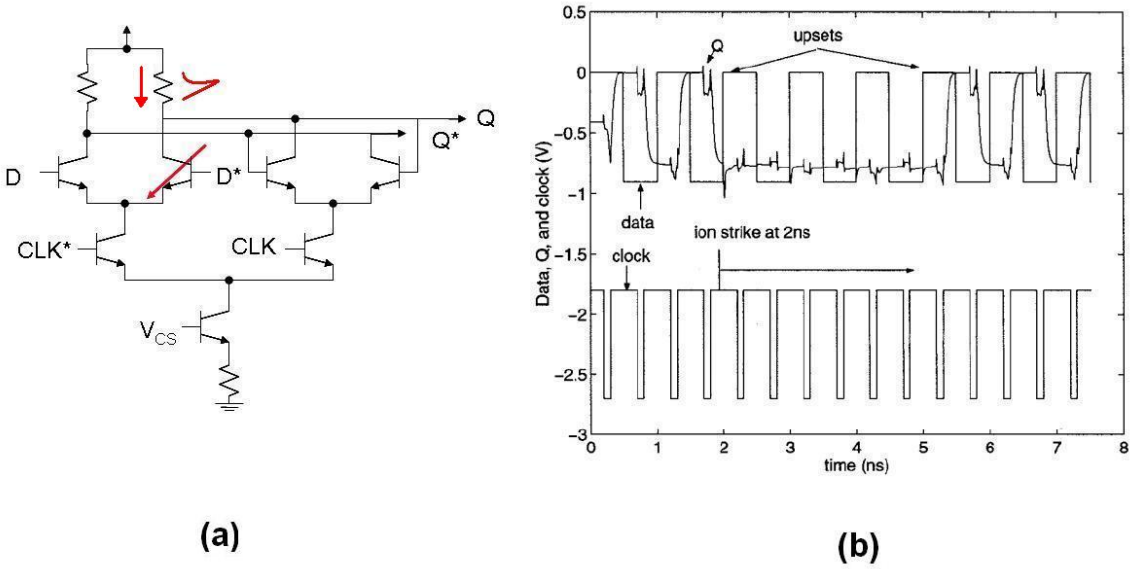


Figure 10: A voltage pertubation induced on one collector terminal coupling forward to result in a digital state flip (After [19]).

can diffuse into and flood a nearby depletion region, shielding electric field lines, and result in a funneling effect. In addition to charge that is initially collected by depletion regions through drift processes, charge which is generated deep into the substrate can diffuse upwards towards junctions and be collected. As generated charges from ion tracks are collected by the depletion regions of a device, transient currents are induced on the terminals of the device. Given transients of sufficient amplitude and duration, significant voltage perturbations may be introduced as these currents flow through nodal impedances. To understand how this voltage perturbation can result in a single/multiple bit upset, a standard bipolar current-mode logic (CML) digital latch (half of a master/slave topology) is considered. As seen in Figure 10 (a), a differential pair controls the direction of current flow through the resistors tied to the collector, while the clocked HBT controls when the input is coupled forward to the output. The positive feedback maintains the previous output of the latch while the input and output are decoupled.

If an ion striking an HBT whose base input is D* is considered when the input D

is logic high and input D* is logic low, the following set of events will take place. The charge generated within the HBT will be collected through the processes mentioned earlier (immediate drift/funneling, and slower diffusion) inducing a current on each of the device terminals. The terminal of interest for this latch is the collector, given that the flow of collector current through the resistor controls the output of the latch. The direction of the transient current flow can be determined by recognizing the carrier type collected at the terminal interior to the device. For NPN transistors (predominant in SiGe BiCMOS platforms due to their inherently higher speeds), the collector is doped n-type, resulting in generated electrons flowing out of the collector. This carrier flow corresponds to a current flowing into the collector. If the amplitude of this transient current is sufficiently high, the voltage drop across the resistor will be large enough to match a digital zero (instead of the expected output of a digital one). If this perturbation occurs during a clock edge, the incorrect logic state will be latched into the cell, resulting in an SEU. If the clock is operating at a high enough frequency, the duration of the current pulse may be sufficient to result in multiple bit upsets, as illustrated in (b) of Figure 10.

A figure of merit that has arisen to correlate particle strike events with a corresponding SEU rate is the critical charge [79]. If the transient current pulse on a device terminal is integrated over the entire duration of the pulse, a quantity corresponding to the total amount induced charge on the terminal is acquired. The integral of the current at which the latch first experiences an upset is defined as the critical charge for the circuit. This variable has been shown to be a highly circuit-specific term whose value and validity strongly depend on the nodal impedances of a device embedded in a circuit [72]. Despite the dependence of critical charge on circuit parameters, understanding charge collection mechanisms of a device and work towards suppression of collection remains fundamental for improving the sensitivity of transistors to SEU.

1.4 Hardness Assurance Testing

In order to guarantee that microelectronic systems destined for orbital and deep-space applications will reliably operate over the intended system lifetime without suffering catastrophic radiation-induced failure or repeated corruption of scientific data, hardness assurance testing must be performed on both the system and component level. Ideally, a system would be tested under identical environmental condtions, or, more appropriately, within the environemnt of the intended application. For space-based systems, testing in the intended environment is unfeasible from a cost, statistics, and timing perspective; therefore, terrestrial-based test facilities must be employed to replicate the dynamic radiation environment of space [74]. Testing guidlines have been established over the years for both total dose (e.g., the U. S. test guideline MIL-STD-883, Method 1019 and the European test guideline BS 22900) and single event testing (e.g., JESD57 and ASTM F1192) [92]). These guildlines set standards in particle energy, flux, dose-rates, bias-states, and annealing times for a wide range of potential radiation experiments. With these guidelines in place, the radiation susceptibility of current SiGe systems can be tested, and new hardening methodologies can be developed and subsequently validated. In the following sections I will summarize some of the most common ion-accelerator/pulsed-laser facilities employed by radiation-test engineers for SEE testing.

1.4.1 Heavy-Ion Broadbeam Facilities

To replicate the heavy-ion species found in space (originating from CGR and solar events) cyclotron facilities provide moderate-energy ion-beam cocktails with variable ion flux. These are spatially unresolved beams (meaning no position-location can be determined for any strike-event) and as such only are used to generate error statistics for systems. This data is typically represented in the form of an event cross-section, where the event is a user-defined criteria for an error event [47]. The event cross is

calculated using (3) where the total accumulated events are dividied by the effective ion fluence of the experiment.

$$\sigma = \frac{Event_{total}}{Fluence_{eff}} \tag{3}$$

As these particle energies are much lower than actual heavy-ion particle energies found in a GCR spectrum, care must be taken to guarantee that the penetration depth of the ion species is adequate to deposit sufficient energy within the semiconductor. Energy loss must be especially considered for any test that is performed in the ambient atmopshere, as significant losses are experienced in just a few centimeters of air. Accordingly, many facilities provide vaccuum chambers to minimize energy loss of incidenct ions. The two heavy-ion broadbeam facilities heavily used for the studies included in this disseration are the Texas A&M University (TAMU) Cyclotron Institute and the Lawrence Berkeley National Lab's (LBNL) 88-inch Cyclotron facility.

TAMU provides users with a wide selection of ion beams encompassing energies of 15 MeV/u, 25 MeV/u, and 40 MeV/u enable testing with LET values ranging from 2.5 MeV-cm^2/mg to 93 MeVcm2/mg at normal incidence. The 15 MeV/u beams include ^{20}Ne,^{40}Ar, ^{63}Cu, ^{84}Kr, ^{109}Ag, ^{129}Xe, ^{141}Pr, ^{165}Ho, ^{181}Ta, and ^{197}Au; the 25 MeV/u beams include ^{20}Ne, ^{40}Ar, ^{84}Kr, and ^{129}Xe; and the 40 MeV/u beams include ^{20}Ne, ^{40}Ar, ^{84}Kr, and protons. Beams are delivered with a high degree of uniformity over a 1.8"1.8" area for samples irradiated in a vacuum and over a 1" diameter for samples irradiated in air [2]. Unlike TAMU, the LBNL facility provides ion beams in the form of "cocktails." These ion cocktails are beams consisting of several heavy ions with the same mass-to-charge ratio. Four standard cocktails are available for radiation-test engineers: 4.5, 10, 16, and 30 MeV/u. Depending on the cocktail, LETs from 1 to 100 MeV-cm^2/mg and flux levels of up to 10^2 ions/cm^2-sec are available, with a beam diameter of 2 inches [1]. The facility operator is able to use the cylcotron frequency to select only the desired ion for DUT irradiation. Both in-air and vacuum capabilities exist; however, with the much lower energies of the LBNL facility, nearly

all broadbeam tests are performed in vacuum.

1.4.2 Heavy-Ion Microbeam and Pulsed-Laser Facilities

A more in-depth analysis of the impact of heavy-ions on circuits requires knowledge of the spatial location of the incident ion. Microbeam facilities provide this capability by generating low-current (0.1-1 fA or $\approx$ 1-10,000 ions) ion beams that can be rastered across device and circuits. Typical measurements for this type of facility included both Ion Beam Induced Charge Collection (IBICC) and Time-Resolved Ion Beam Induced Current (TRIBIC) [10, 90]. IBICC measurements are performed by feeding current pulses originating from an ion-strike into a preamplifier and digitized to calculate the integrated charge. This technique benefits from the ouput being independent of all inductive and capacitive parasitics that may appear in the measurement set-up (conservation of charge) [89]. TRIBIC measures directly capture the induced transient currents using high-speed sampling or real-time oscilloscopes [107]. This technique has long been limited in its applicability by the lack of sufficient measurement equipment to satisfy the stringent demands of the high-frequency transient pulses.

Sandia National Lab's microbeam facility [25] was used for the heavy-ion microscopy studies performed in this dissertation. This facility relies on a High Voltage Engineering EN Tandem van de Graaff accelerator whose maximum terminal voltage is 6 MV. Sputter ion sources (held at ground potential) provide the ions which are stripped of electrons and accelerated by the positive terminal. Nearly any ion species can be accelerated; however, the most common ion beams include ^{12}C (up to 36 MeV), ^{16}O (up to 48 MeV), ^{28}Cu (up to 48 MeV), ^{35}Cl (at 35 MeV), ^{63}Cu (at 50 MeV), and ^{197}Au (up to 100 MeV). The microbeam is focused by imaging object slits using a Martin lens. The minimum beam spot is generally 1 μm (x) by 0.5 μm (y); however, the true value depends on ion species, ion energy, and the tuning of the system.

An alternative to the heavy-ion studies is the use of pulsed-laser for generating

ionized charge within a semiconductor system. Pulsed-laser facilities are advantageous to heavy-ion facilities in the much lower cost of use and the minimization of damage to devices and circuits. Identical to heavy-ion microscopy, both IBICC and TRIBICC studies can be performed in a pulsed-laser environment. There are two types of pulsed-laser measurement benches that one can use to probe circuit sensitivities to radiation, these include front-side single-photon absorption (SPA) tests [63, 64] and back-side two-photon absorption (TPA) [62] tests. These two measurement systems can be described as follows for the Naval Research Laboratory's (NRL) pulsed-laser lab:

1. For SPA measurments, a beam of above-bandgap photons is illuminated on the front-side of a silicon wafer. The absorption of photons by semiconductor systems is well characterized and can be calculated to provide equivalent ion-LETs for a given laser energy [29]. At the NRL, charge generation is accomplished using a cavity-dumped dye laser system capable of generating laser pulses 1.5 ps to 2 ps long with wavelengths ranging from 575 nm to 630 nm and 800 nm to 900 nm generated using the laser dyes rhodamine 590 and styryl 9, respectively, at repetition rates between 1 kHz and 12 kHz [65]. DUTs are irradiated on a motorized stage with 0.1 μm resolution and with optical pulses focused using a 100 X objective, yielding a Gaussian spot size of 1.2 μm at the air-to-material interface. This technique is limited by the overlayers of a circuit, as the laser will be reflected by any metals over the device active area, prohibiting charge deposition.

2. For TPA measurements, sub-bandgap photons are focused such that photon-photon interactions occur allowing simultaneous absorption as if a single photon were of twice the original wavelength. An amplified titanium sapphire laser system (Clark-MXR CPA1000) is used to produce optical pulses at 800 nm

with a repetition rate of 1 kHz and a 120 fs pulse duration. A beta barium borate nonlinear crystal is used to tune the laser output to wavelengths ranging from 1.1 μm to 3.0 μm, which corresponds to photon energies ranging from 0.41 eV to 1.12 eV. Devices are imaged using a Si CCD and are irradiated on a motorized stage at 0.1 μm resolution. The largest challenge (and biggest source of uncertainty) for this technique is the conversion of the laser energy to equivalent ion-LET [91].

1.5 3D TCAD and Mixed-Mode Modeling

While heavy-ion and pulsed-laser experiments generate an important piece of the radiation-effects puzzle, they are unable to provide insight into the physical mechanisms that give rise to transient currents with transistors. To probe this information, it is necessary to turn to 3D Technology Computer Aided Design (3D TCAD) packages. For the studies in this dissertation, Computational Fluid-Dynamic Research Corporation's (CFDRC) NanoTCAD software package was used [85]. This software has the capability of modeling an ion-strike as either a fixed-density gaussian track of charge with a sharp gaussian time profile, or a variable-charge generation path based on Monte Carlo simulations using the Stopping Range of Ions in Matter (SRIM) [111].

Circuit-level SEE simulation can be broken into two general classes: coupled and decoupled. Decoupled techniques attempt to inject known transient current waveforms into the internal nodes of a compact-modeled circuit. This technique is the simplest form of simulation, but does not account for internal feedback mechanisms which may alter the origination of transient currents for the SiGe HBT ¡insert reference¿. A more sophisticated approach is to combine the compact-modeled circuit with a 3D TCAD platform. This technique is known as fully-coupled mixed-mode 3D TCAD modeling, and has been used often in the literature to provide a holistic view of the complex device-circuit interactions encoutered with SEEs [104, 103, 102, 68]. By replacing a

single device in the circuit with a multidimenisional TCAD model, the dynamic shifts in terminal biases and impedances can be captured over the evolution of the ion-strike. This technique provides a more accurate picture of the generation and propagation of transient currents for a circuit, but comes with the drawback of increased computation complexity and simulation time.

1.6 Research Objectives

Field-effect transistor technologies have been critical building blocks for satellite systems since their introduction into the microelectronics industry. The extremely high cost of launching payloads into orbit necessitates systems to have small form factor, ultra low-power consumption, and reliable lifetime operation, while satisfying the performance requirements of a given application. Silicon-based complementary metal-oxide-semiconductors (Si CMOS) have traditionally been able to adequately meet these demands when coupled with radiation hardening techniques that have been developed over years of invested research. However, as customer demands increase, pushing the limits of system throughput, noise, and speed, alternative technologies must be employed. Silicon-germanium BiCMOS platforms have been identified as a technology candidate for meeting the performance criteria of these pioneering satellite systems and deep space applications, contingent on their ability to be hardened to radiation-induced damage. Given that SiGe technology is a relative new-comer to terrestrial and extra-terrestrial applications in radiation-rich environments, the same wealth of knowledge of time-tested radiation hardening methodologies has not been established as it has for Si CMOS. The incorporation of SiGe BiCMOS technologies in systems destined to operate in space-based platforms promises to provide a multitude of advantages over standard silicon technologies. These advantages stem from silicon germanium's inherent excellent cryogenic performance which enables cold electronics (the exclusion of "warm boxes" for containing electrical systems in space), as well as

its built-in multi-Mrad total dose immunity. Although SiGe BiCMOS technology has been experimentally proven to be inherently tolerant to total-ionizing dose damage mechanisms, the single event susceptibility of this technology remains a primary concern. The objective of this research is to characterize the physical mechanisms that drive the origination of ion-induced transient terminal currents in SiGe HBTs that subsequently lead to a wide range of possible single event phenomena. Building upon this learning, a variety of device-level hardening methodologies are explored and tested for efficacy in the context of device and circuit implementations.

CHAPTER II

RADIATION-INDUCED TRANSIENT ORIGINATION IN SIGE HBTS

As was discussed in the previous chapter, the passage of highly-energetic charged particles through a semiconductor system will result in the creation of a wake of freely ionized charge carriers along the trajectory of particle. The subsequent "collection" of these charges gives rise to the plethora of single event effects that can disrupt system operation or potentially cause catastrophic failures. All of the single-event phenomena, regardless of their system impact, manifest from the creation of radiation-induced transient currents on the terminals of a transistor. It follows that a detailed understanding of the origination of single event transients for any device will be paramount for interpreting system impact and developing effective radiation hardening methodologies.

Before delving into the detailed physics of transient origination in SiGe HBT transistors, it is worthwhile to discuss the foundations of this field of study, as well as discuss commonly misused terms and concepts. The most important misconception in the field of radiation effects is the concept of "collected charge" [23]. Although the movement of free charges is the underlying mechanism that gives rise to transient terminal currents, this current does not appear only at the instant that the charge crosses the threshold of an ohmic contact. Instead, transient currents are induced as result of the instantaneous change in the electrostatic flux lines that terminate on an electrode. The flow of charges through an electric field in any medium therefore "collects" the charges onto the device terminal; however, it should again be stressed that this current is not the amount of charge received by the electrode per second.

Instead of the term "collected charge," the term "induced charge" is much more physically correct; however, with the current heavy usage of "collected charge" in the radiation-effects community, these two phrases will be used interchangeably.

The study of the induction of current on electrodes arising from moving charges in the presence of electric fields was first pioneered for the optimization of radiation detectors [34] and the characterization of current transport in vacuum tubes [86, 93]. From these works the Ramo-Shockley theorem was created, which generally defined the instantaneous electric current induced by a point charge traveling in the vicinity of multiple electrodes [38]. For a one dimensional case of two parallel electrode plates separated by a fixed distance, d, with a moving point charge q, traveling a distance of Δx, the Ramo-Shockley theorem predicts the induced charge ΔQ to be given by:

$$\Delta Q = q * \frac{\Delta x}{d}. \tag{4}$$

The transient current induced on the electrode $I(t)$ can then be calculated from (5) using the carrier velocity $v[x(t)]$ by

$$I(t) = q * \frac{v[x(t)]}{d}. \tag{5}$$

This work formed the foundation for future expansions of the theory, most noticeably by Gunn in 1964 who extended the analysis to include the general expression for any arbitrary arrangement of charges and electrodes [30]. The theories that have been described to this point are built upon the framework of several underlying assumptions that need to be addressed [10]. These assumptions include:

1. A negligible perturbation in the electric field lines within the semiconductor device occurs due to the excess charge concentration ionized by a particle.

2. There is an instantaneous propagation of the electric field.

3. The device terminals (electrodes) are connected to ideal voltage sources such that carrier motion does not perturb the potential of the electrode.

It will be important to keep these assumptions in mind as we move forward with the analysis at hand. The characterization of radiation-induced terminal currents in any semiconductor platform has typically been performed through the measurement of induced charges on device terminals for a circuit-relevant bias condition, using the IBICC set-up described in Chapter 1. With the maturation of high-speed, real-time, digital sampling oscilloscopes (DSOs), measurement capabilities have evolved to allow direct-capture of transient current waveforms (TRIBICC measurements) which provide much deeper insight into the driving physical mechanisms. Coupling this experimental data with calibrated 3D TCAD platforms can further enhance the learning. Recently, heavy-ion microbeam and broadbeam TRIBICC measurements of first-generation SiGe *npn* HBTs have been published [76]. This study experimentally illustrated several key concepts behind current understanding of SiGe HBT SEE sensitivity; however, a complete explanation for the origination of SETs in these devices is not provided.

The current body of work seeks to complete the understanding of SET origination in SiGe HBTs through both experimental analysis as well as calibrated 3D TCAD modeling. Two baseline model decks, calibrated for IBMs first generation 5AM technology (one bulk, the other SOI), are used as the reference point for all of technology extensions performed (scaling, doping, bias, etc.). Our studies are focused on the *npn* SiGe HBT. The analysis begins with a look into the dependence of strike location on the transient terminal currents induced on the SiGe HBT for both the bulk and the SOI technology platforms for normal incidence particle-strikes. This study is followed with a discussion of the impact of the angle of incidence of the energetic particle. Moving forward, the impact of terminal bias and particle energy is investigated. Using the SOI model deck (identical doping profile to the original bulk deck), the impact of technology scaling is explored with modulations to the doping profile and germanium profile. Finally, fully-coupled mixed-mode TCAD simulations are used as a tool to illustrate circuit-specific sensitivity to the transient currents

that have been discussed. From this analysis, the framework for device-level radiation hardening methodologies are formed, which are covered in the remaining chapters.

2.1 Strike Location

Radiation-interaction with semiconductors in a space environment is governed entirely by probability (as is all of nature). The likelyhood of a particle passing through any specific region of a SiGe HBT is of equal probability for every possible strike location for a system in geosynchronous orbit. As such, it is necessary to investigate the transient currents that are induced for all possible particle-strike locations. Three distinct regions of a SiGe HBT in a bulk technology and are isolated for study. Similarly two distinct regions are identified for a SiGe HBT in an SOI technology. Particle-strikes through these regions are illustrated in Figure 11, which shows a top-down view of a SiGe HBT from both technology platforms. The strike locations of interest include the emitter area, the external active area within the confines of the deep trench, and through the substrate external to the deep trench isolation for a SiGe HBT in a bulk technology. For the SOI technology, the external deep trench isolation strike is omitted, as the deep trench typically extends all the way to the buried oxide in these platforms, providing near-perfect isolation.

The three regions have been broken down based upon the number of metallurgical junctions that a normally-incident particle will encounter during its transit through the semiconductor. For a particle strike through the emitter area of a bulk SiGe HBT, the ion will pass through the emitter-base, collector-base, and subcollector-substrate junctions. Similarly, for an SOI HBT the particle will pass through the emitter-base and collector-base junction. This particle strike location is considered to be a worst-case strike, as all possible junctions are encountered [75]. The second region encompasses the area internal to the deep trench that is external to the emitter area. For a bulk platform, a particle will only pass through the subcollector-substrate

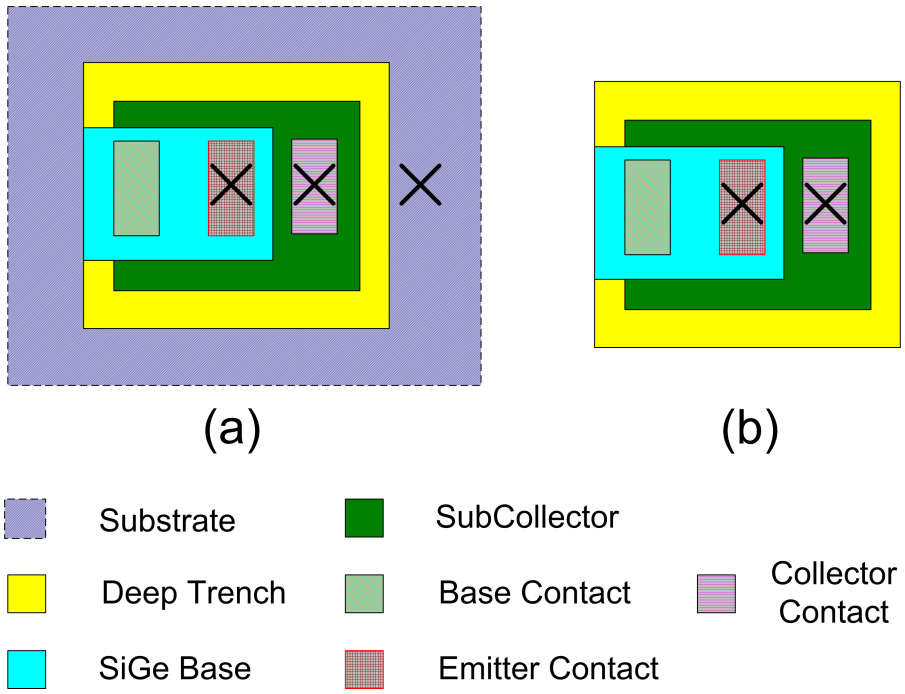


Figure 11: Top-down cartoon view of the bulk SiGe HBT and SOI SiGe HBT modeled devices. The investigated strike locations for ions at normal incidence are shown with X's.

junction in this region, whereas in an SOI platform no junction is encountered. The final region encompasses strikes through the substrate, external to the deep trench for a bulk platform. No junctions are penetrated for particle strikes in this region; however, ionized charge in the particle track can potentially diffuse to the subcollector-substrate depletion region and induce transient currents [78, 77]. To perform the analysis, normally-incident ion-strike simulations were executed for a fixed position of all of the regions defined previously, for both the bulk and SOI model deck. The modeled device had an emitter area of 0.50 x 2.15 μm^2 and an internal deep trench area of 4.25 x 4.00 μm^2. A fixed transistor bias was chosen of 1 V on the collector and 0 V on all other terminals. A fixed ion LET of 10 MeV-cm^2/mg was selected. The impact of varying transistor bias and ion energy will be developed in later sections.

2.1.1 Emitter-Center

The simulated ion-induced transient current waveforms for all device terminals for a 10 MeV-cm^2/mg particle strike through the center of the emitter terminal for both a bulk *npn* SiGe HBT and an SOI *npn* SiGe HBT are shown in Figures 12 and 13, respectively. Although the generation of transient currents is an aggregate event, various mechanisms will dominate the current profiles at different times. For a bulk SiGe HBT, the ion-induced transient waveforms can be broken into three distinct regions. For SiGe HBTs fabricated in an SOI process, only two regions are applicable. The understanding of the physical origins of the ion-induced transient currents for each of these regions will prove to be crucial for future studies of device-level radiation hardening techniques.

From the formulation of the Ramo-Shockley theorem described earlier, free carriers

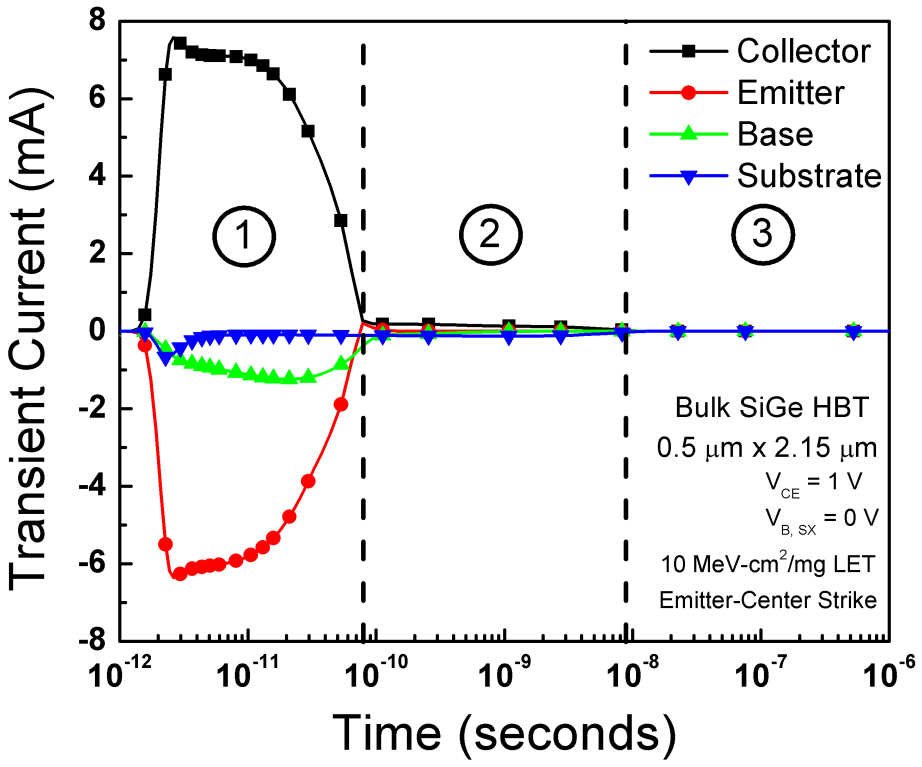


Figure 12: Simulated ion-induced transient current waveforms for all devie terminals of a bulk *npn* SiGe HBT for an emitter-center strike.

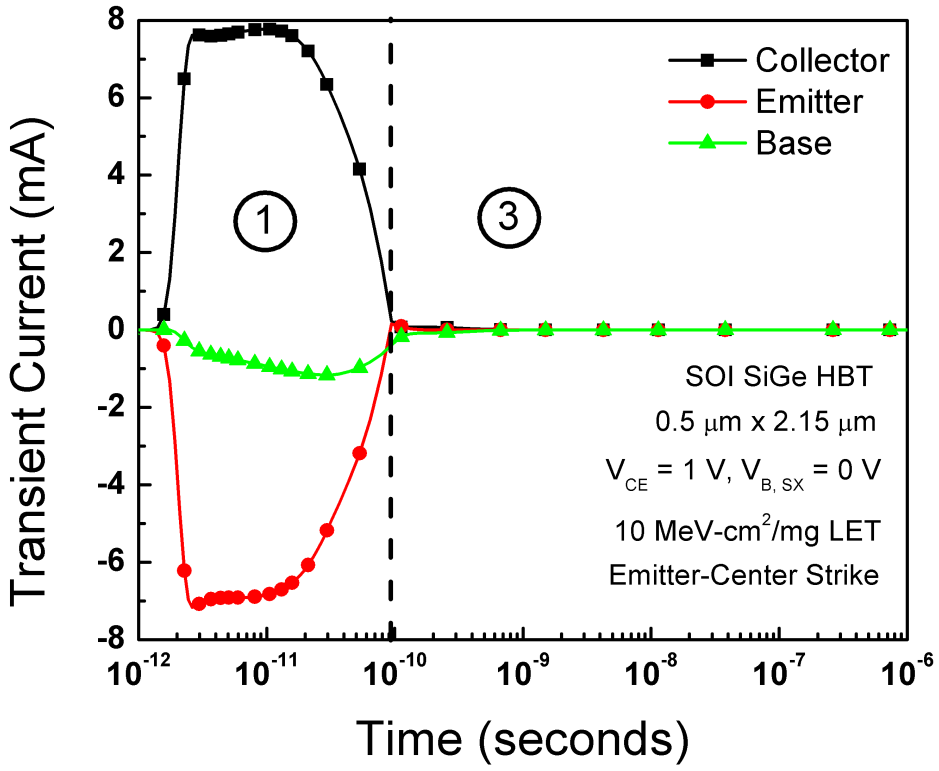


Figure 13: Simulated ion-induced transient current waveforms for all device terminals of an SOI *npn* SiGe HBT for an emitter-center strike.

generated in the depletion region of an HBT will be separated by the electric-field lines of the junction and drift to the respective n and p-type neutral regions. Specifically, ionized electrons will drift to the neutral n-type region while the ionized holes are pulled into the p-type region. The magnitude and duration of the transient waveforms will be dependent on the width of the depletion region and the strength of the electric-field lines. Based upon this understanding it would be expected therefore that the polarity of the transient currents induced for similarly doped regions will be identical, with the collector transient much larger in magnitude and longer in duration. However, the collector and emitter terminal currents of Figures 12 and 13 are found to be opposite in polarity and nearly identical in magnitude and duration for region 1. To understand this discrepancy with the Ramo-Shockley theorem, it is necessary to re-examine the assumptions that the form the framework of the theory.

One of the underlying assumptions of the Ramo-Shockley theorem is that the

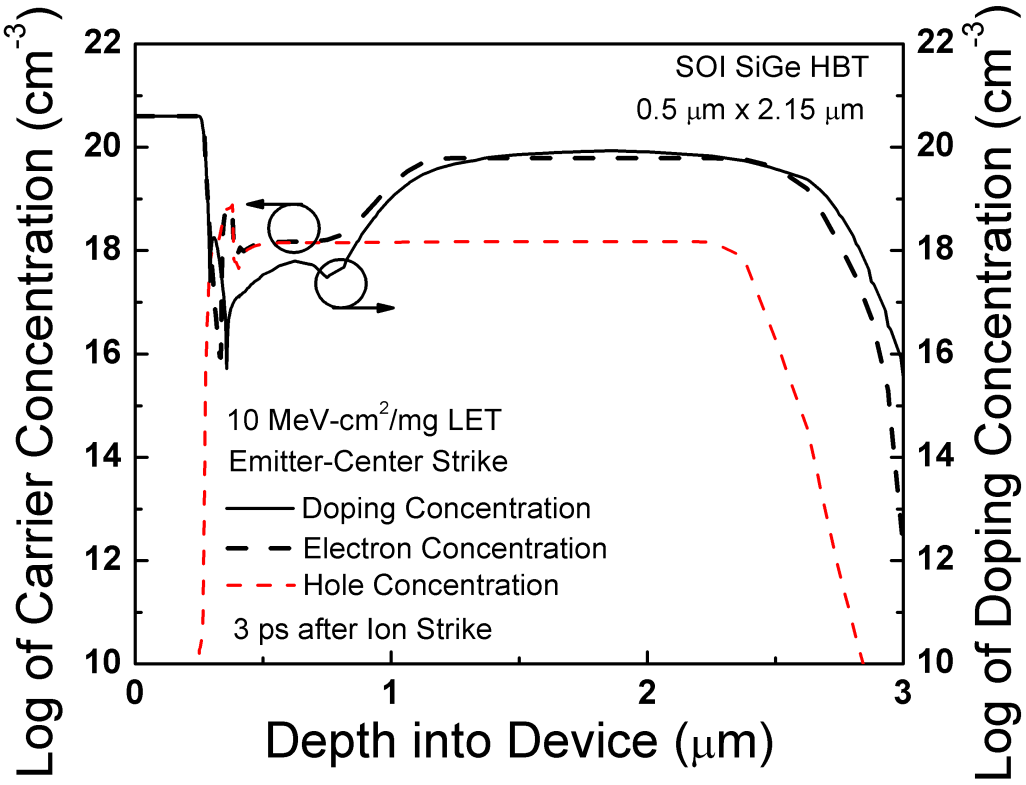


Figure 14: Excess free carrier concentrations and doping profile, extracted through a vertical cut through the center of a bulk SiGe HBT, plotted as a function of depth into the modeled device. The calculation was performed 3 ps following a simulated 10 MeV-cm^2/mg ion strike.

induced carrier concentration does not perturb the existing electric field structure within the depletion region. The ionized carrier concentration for a simulated SiGe HBT struck with a 10 MeV-cm^2/mg ion is over-layed with the background doping through a vertical cut through the center of the transistor in Figure 14. The concentration was calculated 3 ps following a simulated ion-strike. The energetic particle induces an initial ionized charge distribution with a peak value of approximately 10^{18} cm^{-3} through the ion track. Ionized charges quickly begin to separate with holes accumulating in the base region of the transistor. This accumulation generates a free carrier concentration that is comparable to the fixed-charge density of the base-side depletion regions of the emitter-base and collector-base junctions. Similar to the Kirk effect [44], this mobile charge shields the electric fields lines in the depletion region, resulting in a collapse

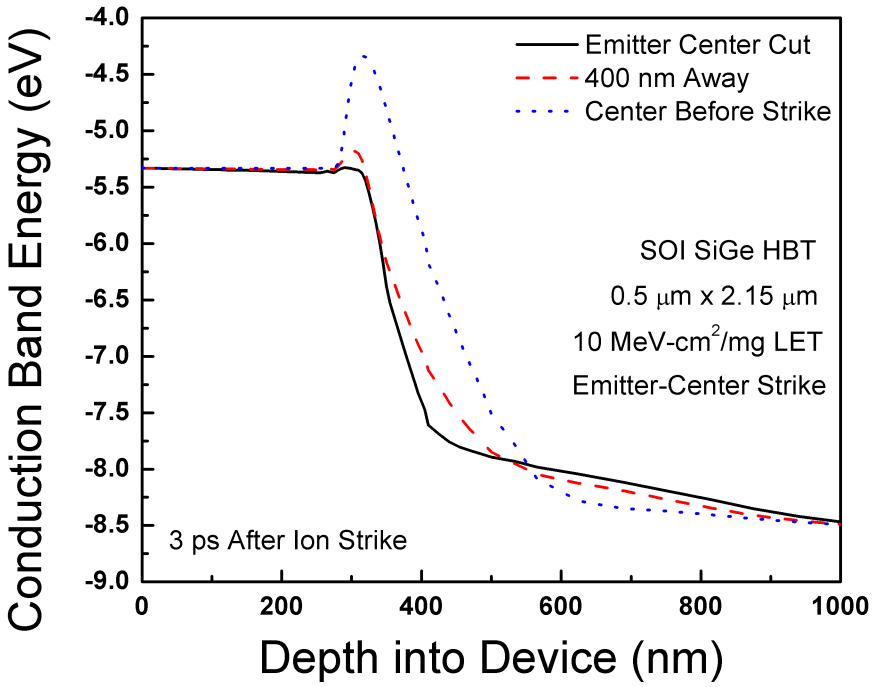


Figure 15: Conduction band energy levels plotted as a function of depth into a modeled bulk SiGe HBT for two lateral positions, the emitter-center and 400 nm away from the center.

of the junction and a push-out of the electric field lines into the neutral regions of the SiGe HBT. In the literature, this effect has been described classically as funneling [61], or more accurately potential-modulation [20], when a single p-n junction is under consideration. The stacked multi-junction structure of the HBT, however, results in a large forward bipolar current when the depletion regions collapse, assuming a non-zero V_{CE} is present.

The conduction band edges through the center of the ion path and at a lateral distance of 400 nm away from the center are plotted in Figure 15 as a function of depth into the device. Prior to the ion-strike, the strong emitter-base energy barrier is clearly present; however, directly following the strike, the collapse of the barrier in the strike center is evident. This is a localized collapse, with the energy bands still intact at lateral distances greater than 400 nm away from the strike center. The collapse of the conduction band energy barrier results in electrons being injected from emitter into

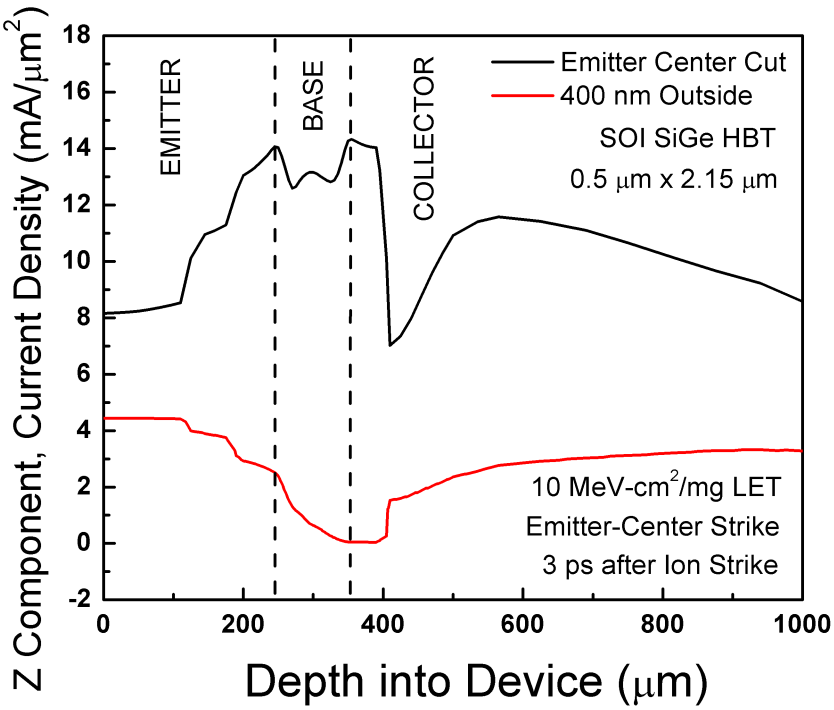


Figure 16: Z-component of the current density, J_z, plotted as a function of depth into a modeled bulk SiGe HBT for two lateral positions, the emitter-center and 400 nm away from the center.

the base, in a fashion synonymous with forward bipolar transfer current. Although the conduction band barrier is substantially reduced at 400 nm, the current electron current profiles in the transistor indicate that electron flow is primarily constrained to the ion-track center, where the band edges have been completely nullified, as illustrated in Figure 16.

Previous investigations of stacked p-n junctions, from the context of triple-well CMOS processes, have described this effect as an ion-induced resistive shunt path [33, 46, 45]. This nomenclature is misleading; however, as standard forward-mode operation of a bipolar transistor resembles a low resistive path from the emitter to the collector terminal. This shunt path is localized to the strike area and dynamically changes in width and resistivity over time in a complicated manner that is a function of both applied bias and ion strike angle. Although the transient current of the emitter and collector contacts reflects bipolar action between these terminals, the

base transient current originates from a completely separate process. For normal bipolar action, holes flow into the base contact to compensate for the injection of holes into the emitter. For a particle strike, the ionized hole concentration supplies the necessary back-injection of holes into the emitter to compensate for the collapse of the energy bands. The remaining ionized holes are swept out of the base through the base contact, resulting in the base transient current.

The onset of region 2 in Figure 12 (and likewise region 3 in Figure 13) marks the end of the ion-induced shunt transient. The ionized carrier concentration has fallen below the background doping density, allowing the depletion regions of the emitter-base and collector-base junctions to reestablish, cutting off the forward bipolar current that was present [46]. For both the bulk and SOI SiGe HBT, the emitter transient current reverses polarity following the collapse of the shunt, as the remaining ionized elections in the reformed emitter-base region are swept across the electric field lines. The collector and substrate transient currents however remain substantial, as the ionized carrier concentration is still larger than the background doping of the substrate, maintaining a collapsed subcollector-substrate depletion region. The electric field lines extending into the substrate result in a drift transport of charges induced deep in the substrate. This region of the transient current is not present for the SOI HBT, as the subcollector-substrate junction is removed by replacing the substrate with the buried oxide. The final region of the transient waveforms, region 3, marks the recovery of all of the depletion regions of the HBT. Remaining ionized charges are separated by the field lines of the junctions, and transient current origination is driven by the Ramo-Shockley theorem. This current is much lower in magnitude than the shunt-induced currents and is not visible when plotting the transient current on a linear y-scale, as in Figure 12 and Figure 13.

2.1.2 Outside Active Area

The simulated ion-induced transient current waveforms for all device terminals for a 10 MeV-cm2/mg particle strike through the collector contact for both a bulk *npn* SiGe HBT and an SOI *npn* SiGe HBT are shown in Figures 17 and 18, respectively. The ion track for this strike does not pass through the intrinsic vertical structure, but only passes through the collector (and substrate for a bulk platform). Using the same region-number scheme as for emitter-center strikes transients; these external active area transient waveforms can again be delineated by the mechanisms that drive the origination of the transient current. For the bulk SiGe HBT, two regions, region 2 and region 3, are present. In the SOI SiGe HBT, only region 3 can be identified.

Once again, region 2 is dominated by the collapsed subcollector-substrate depletion region that gives rise to the sustained transient current on the collector and substrate contacts. Once the carrier concentration drops below the background doping of the substrate, the junction re-establishes and the transient current is the result of carrier separation by the field lines of the reformed junction. Neither the base nor the emitter terminal show substantial transients for the bulk SiGe HBT, as the subcollector-substrate junction collects nearly all the excess ionized charge. For the SOI SiGe HBT, the substrate is not present and the collector is confined within the deep trench. All excess ionized charge must either recombine within the neutral collector, or diffuse to the collector-base depletion region. As can be seen from the transient waveforms of Figure 18, only small base and collector current transients result from the collection of the confined excess charge in the neutral collector. This difference between bulk and SOI technologies will be seen in a future section to have important consequences for SEE.

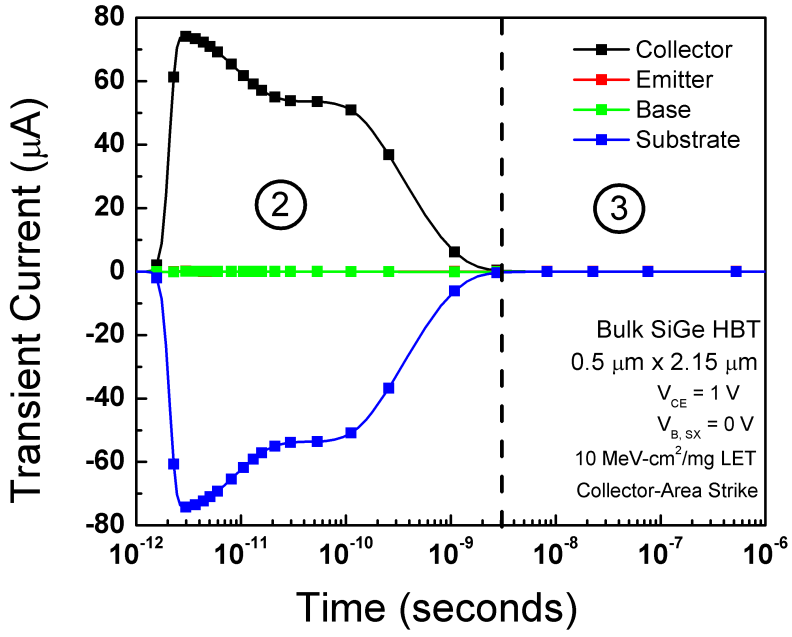


Figure 17: Simulated ion-induced transient current waveforms for all device terminals of a bulk *npn* SiGe HBT for a collector-area strike.

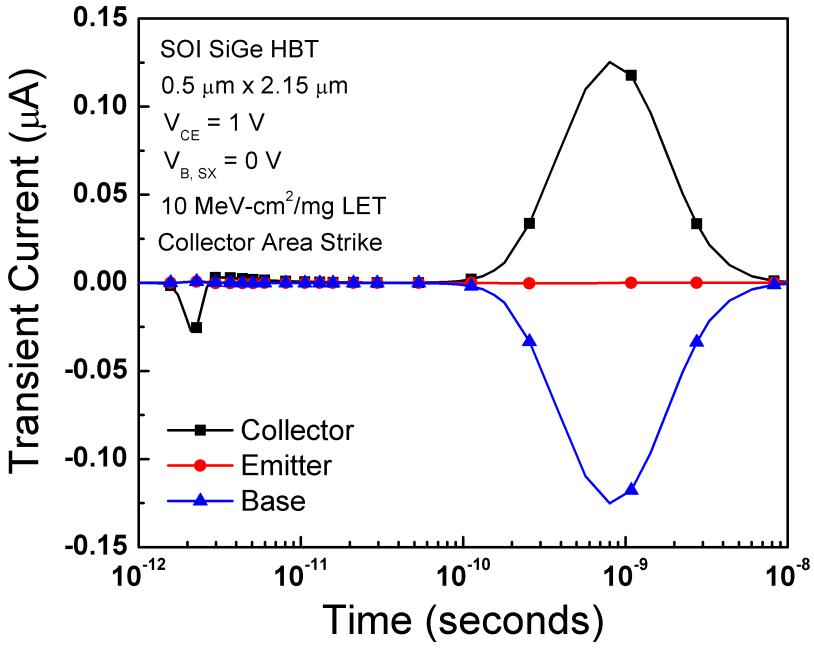


Figure 18: Simulated ion-induced transient current waveforms for all device terminals of an SOI *npn* SiGe HBT for a collector-area strike.

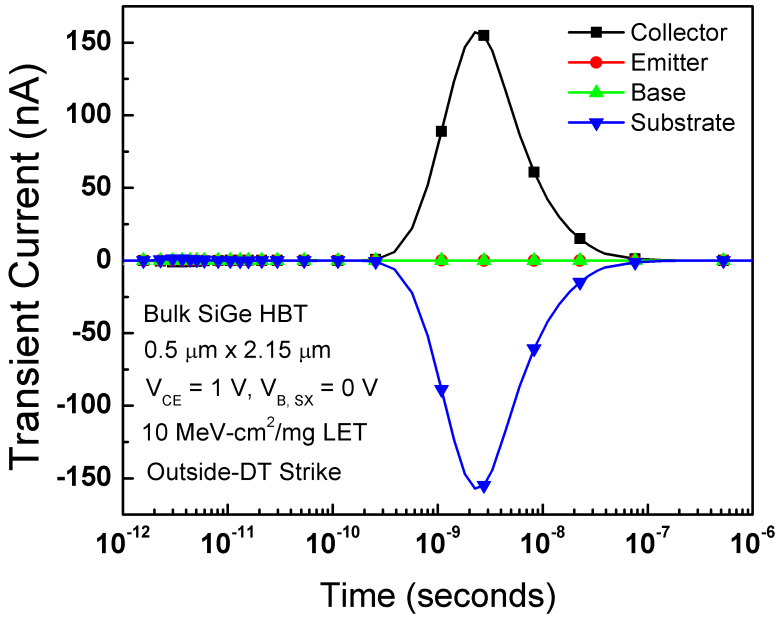


Figure 19: Simulated ion-induced transient current waveforms for all device terminals of a bulk *npn* SiGe HBT for an ion-strike directly outside the deep trench isolation.

2.1.3 External Deep Trench

The simulated ion-induced transient current waveforms for all device terminals for a 10 MeV-cm^2/mg particle strike directly outside the deep trench for a bulk *npn* SiGe HBT is shown in Figure 19. For particle strikes through the substrate, excess ionized charge must diffuse to the subcollector-substrate junction to generate transient currents. With the low background doping of the substrate (10^{15} cm^{-3}), the diffusion length of carriers is large, resulting in substantial quantities of carriers diffusing to the subcollector-substrate junction before experiencing recombination events. This results in a delayed current-pulse on the collector and substrate terminals as shown in Figure 19. Once again the base and emitter terminals exhibit no transient signatures, as no excess carriers encounter the collector-base or emitter-base junctions. For SOI technologies, it can immediately be seen that the total sensitive area of the bipolar transistor is reduced, as the deep trench isolation provides confinement of the sensitive transistor junctions.

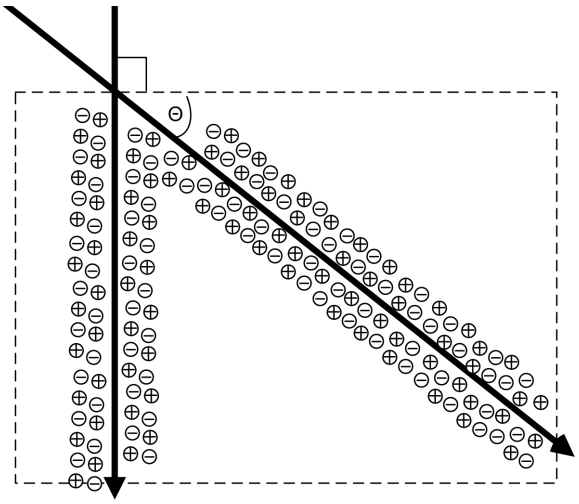


Figure 20: Cartoon of two varied angled ion strikes through a sensitive volume, illustrating the difference in deposited energy.

2.2 Angle Of Incidence

For systems operating outside of near-Earth orbits (geosynchronous/geostationary orbits and deep space probes), the radiation present in the space environment is isotropic in nature. In an isotropic environment, half of the particles will be surface incident at angles below 60 degrees and half will be incident at angles greater than 60 degrees. As such it is necessary to analyze the impact of oblique and grazing ion angles on the impact of transient current origination. Focus is often placed on normally incident particles (perpendicular to the plane of the semiconductor) for experimental studies, as some particle-accelerator facilities are limited in their ability to expose packages at well characterized angles.

A general model for characterizing the impact of angled ion strikes is to adjust the LET of the particle to account for the increase in deposited energy within a given sensitive volume. Figure 20 illustrates this effect, where a physical sensitive volume of fixed dimension is struck by two particles of similar energy at normal incidence to the surface and a grazing angle of θ. To account for the change in path length of the particle through the sensitive volume (and correspondingly greater deposition of

charge in the volume) an "effective LET" is assigned to the particle defined through the law of cosines as

$$L_{eff} = \frac{L}{\cos\theta}. \tag{6}$$

Where L is the LET of the particle at normal incidence and θ is the angle of incidence. This model has been shown to be less applicable for SiGe HBTs, where the deep trench isolation truncates the sensitive volume, complicating the dynamics of junction charge collection ¡reference¿. Given the vertical structure of the sensitive volume of the SiGe HBT, angled particle strikes can pose a worst-case scenario, where much larger quantities of charge will be deposited for equivalent ion LETs.

To illustrate the impact of angled ion-strikes, varying angled ion-strike simulations were executed using the SOI SiGe model deck. The strike path was fixed to pass through the center of the base of the HBT, in the direction of the maximum length of the emitter window to emulate worst-case conditions. The angle is measured in reference to the plane of the surface of the emitter; therefore, a normal incidence ion has a strike angle of 90 degrees while a 0 degree angle is in the plane of the emitter surface. The ion LET was fixed at 10 MeV-cm^2/mg for all simulations. The terminal biases for the simulation included 1 V on the collector, and 0 V on the emitter and base. In Figure 21 the resulting collector current transients for the varying strike-angle simulations are plotted as function of time. While there is a considerable shift in the peak transient current magnitude with decreasing strike-angle, there is no change in duration of the ion-induced shunt. The increase in the transient magnitude is linked to the larger volume of the intrinsic device that experiences a collapse of the energy bands, generating the ion-induced shunt. Although a greater quantity of charge is deposited within the base volume of the SiGe HBT, the density of the excess charge remains identical for all strike-angles. This consistency in the charge density maintains fixed durations for equilibrium conditions to be restored for the energy bands to re-align, shutting down the ion-shunt process.

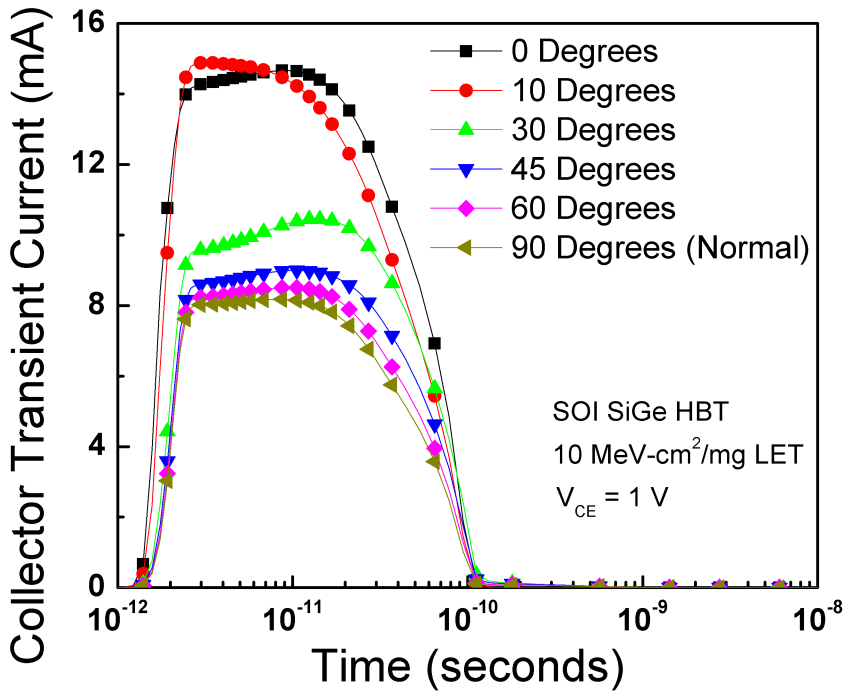


Figure 21: Collector current transients induced from varying angle strikes through the center of an SOI *npn* SiGe HBT.

2.3 Impact of Collector Terminal Bias and Ion Energy

Up to this point, ion-strike simulations have been performed with a fixed bias of 1 V on the collector node. From the analysis of the ion-induced shunt current it has been demonstrated that the collector-to-emitter voltage, V_{CE}, will have a very important influence on the ion-induced terminal currents of an HBT. Also, given the importance of the difference in the ion-induced excess carrier concentration with the background doping of the transistor, the energy of the radioactive particle is expected to play another important role in determining the SiGe HBT transient terminal current origination.

2.3.1 V_{CE} Dependence

With the collapse of the reverse-biased collector-base junction, the applied collector-to-emitter voltage drop must be maintained within the internal device. The applied voltage is balanced through the push-out of the electric field lines of the collapsed

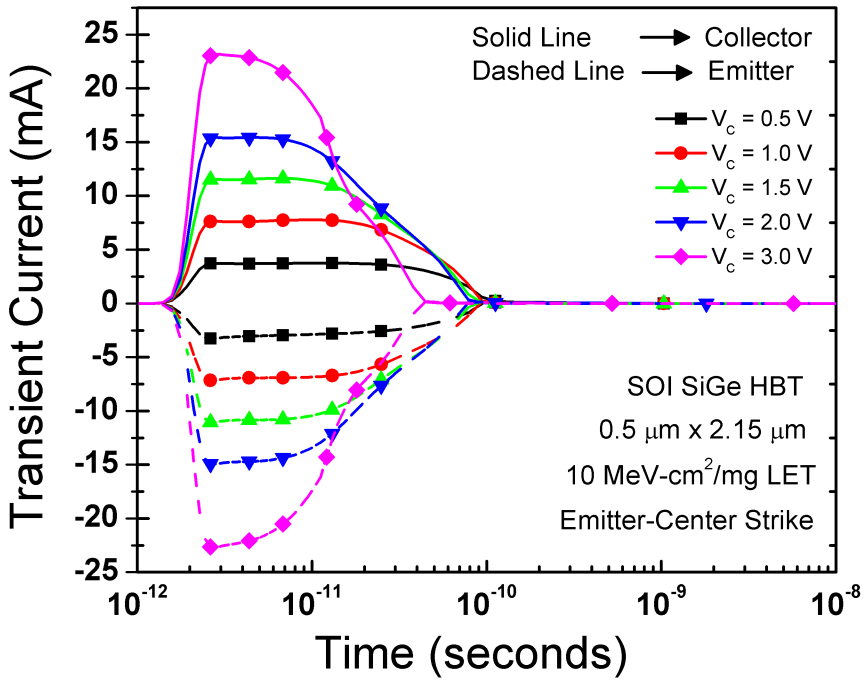


Figure 22: Collector current transients for varying V_{CE} bias, for fixed energy ion-strikes through the center of an SOI *npn* SiGe HBT.

depletion region, which modulates the internal potential of the device pushing it into forward-mode operation. With increasing applied bias to the collector (or equivalently to the emitter), larger electric field lines must be displaced into the neutral regions of the SiGe HBT, resulting in larger drift transient currents. To simulate this effect the bulk first-generation SiGe HBT model deck was employed, using multiple collector biases for a fixed ion-strike through the emitter-center with an ion LET of 10 MeV-cm^2/mg. The collector transient currents induced from these simulations are plotted in Figure 22.

As seen in Figure 22, an increase in the collector bias results in a considerable increase in the peak current transient magnitude. This increase is attributed to the larger electric fields distributed through the neutral base following the collapse of the collector-base junction, which drives the internal potential of the base up. This increase in electric field strength distributed across the base is also seen to have another important impact on the transient current waveform. Specifically, the duration of

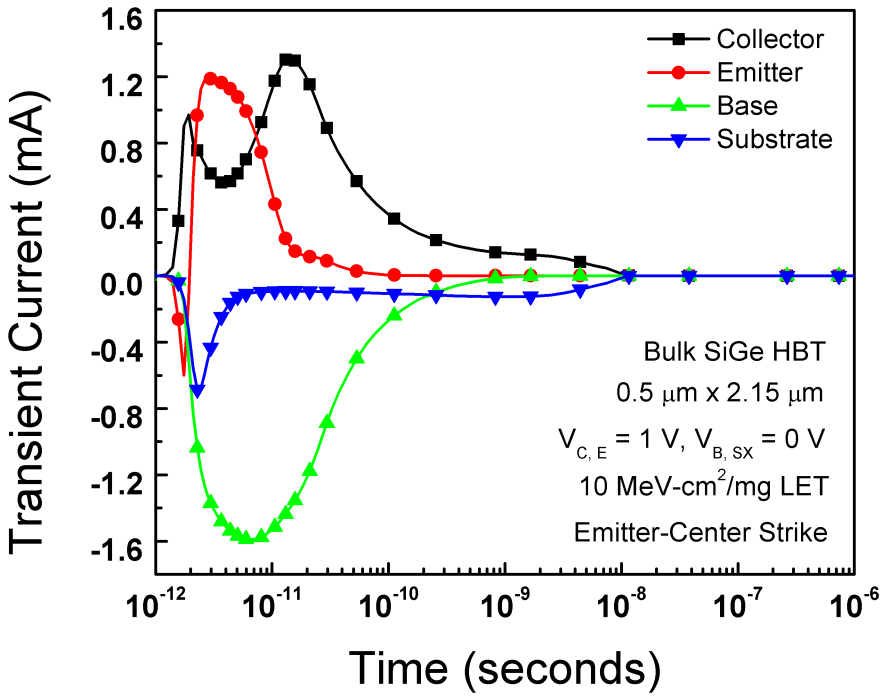


Figure 23: Transient terminal currents induced for an SOI *npn* SiGe HBT biased with 1 V on the collector and emitter.

the ion-induced shunt is found to be reduced as the collector bias is increased. With stronger electric field lines distributed through the active area of the transistor, ion-induced excess carriers are more quickly separated and pulled out of the active area. This effect drops the excess carrier concentration below the background doping level of the base more quickly, shutting down the ion-shunt process.

To illustrate the importance in the voltage differential between the collector and emitter terminals for the ion-shunt effect, another simulation was initiated. For this simulation a bias value of 1 V was placed on both the collector and the emitter terminals while the base terminal was held at 0 V. An ion-strike through the emitter-center of the device was simulated using an ion LET of 10 MeV-cm^2/mg. This bias strongly reverse-biases both the emitter-base and collector-base junctions but maintains a zero voltage differential across the collector and emitter. The resulting transient currents for all device terminals of the SiGe HBT are plotted in Figure 23, and show a remarkably different signature than previous simulations with a finite

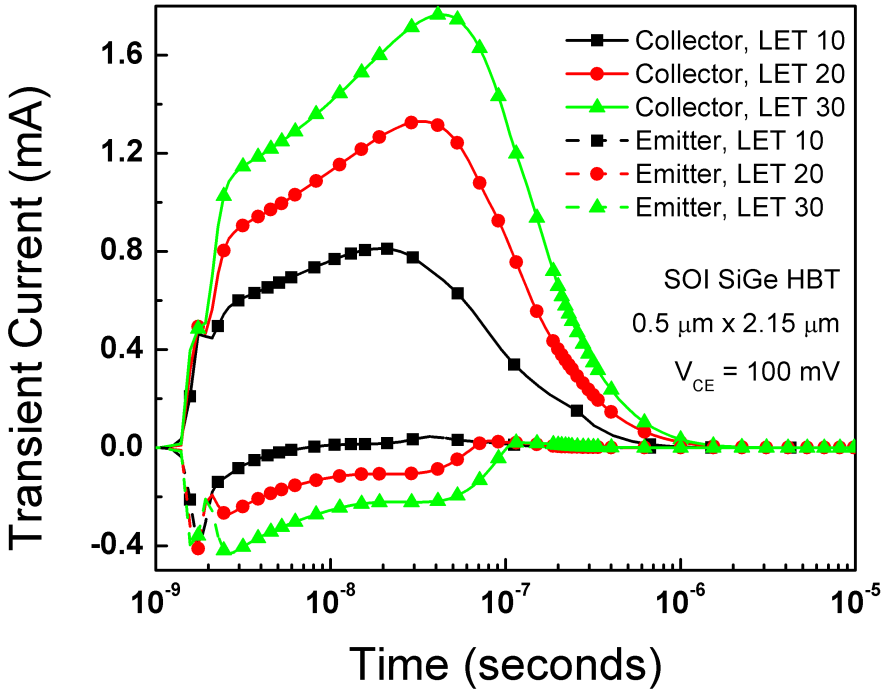


Figure 24: Transient terminal currents induced for an SOI *npn* SiGe HBT biased with 1 V on the collector and emitter.

VCE. Specifically the ion-induced shunt that generates electron flow between emitter and collector is not activated. Instead, a transient profile consistent with standard charge collection physics (similar polarities for collector and emitter signals, with an opposite polarity on the base). Although both the emitter-base and collector-base depletion regions collapse from the flood of ion-induced excess carriers, the lack of a voltage differential prevents any electron injection from emitter to collector. This is synonymous to the standard operating features of a bipolar transistor, where no applied V_{CE} results in minimal transfer current regardless of applied base bias. The presence of the long duration subcollector-substrate transient is still evident in this simulation, as this junction maintains its reverse bias.

2.3.2 LET Dependence

The energy of the incident particle determines the density of ionized excess carriers in the wake of the particle path. Higher energy particles experience less interaction with

the semiconductor lattice, resulting in less energy deposition and a correspondingly lower LET. With the previously discussed importance of the difference in the ion-induced excess carrier concentration and the background doping of the transistor, the density of ionized excess charge (LET) is expected to have an important role in determining the shape of the transient current waveforms. To explore this dependence, the SOI SiGe model deck was employed, with multiple emitter-center ion-strike simulations, executed with varying ion LETs. Ion LETs of 10, 20, and 30 MeV-cm^2/mg were explored. The SiGe HBT was biased with 100 mV on the collector terminal and 0 V on the emitter and base terminals. The collector and emitter transient current waveforms arising from these simulations are plotted in Figure 24. At this low VCE, the ion-induced shunt has a very small impact on the transient currents for the 10 MeV-cm^2/mg. This fact is best illustrated with the emitter current transient, which reverses transient current polarity nearly immediately following the strike event for the minimum LET simulated. As the particle LET is increased, the duration of the ion-induced shunt is seen to likewise increase. A greater density of ionized excess charge in the transistor sustains the collapse of the reverse-biased collector-base depletion region for a greater period of time.

2.4 Impact of Technology Scaling

SiGe BiCMOS technologies have matured as competitors to III-V platforms for wireless applications as a result of aggressive technology scaling [41]. Classical scaling incorporates reductions to both the lateral and vertical physical dimensions of a device coupled together with increases in the vertical doping profile. SiGe HBTs have also been subject to non-classical scaling, including modifications to the device architecture (raised extrinsic base, self-aligned poly-emitter), new dopants (carbon doping), and structural changes to the germanium profile [18]. This large array of changes to the device structure warrants reexamination of the radiation sensitivity of the SiGe HBT

for each new technology generation. Previous work has characterized the impact of technology scaling in the context of TID damage; however, no current work has been performed on identifying the impact of scaling on the single event sensitivity of SiGe HBTs [98].

In the following sections we explore this problem with the aid of 3D TCAD analysis. A first-generation SiGe HBT from an SOI platform is used as the starting point for the scaling study. The SOI model deck is used as it minimizes the total number of mesh nodes as compared to a bulk model deck, which significantly reduces computation time. The topic of scaling also primarily impacts the active intrinsic area to the device. The subcollector-substrate junction essentially scales only in volume with increasing technology generation. In the following sections we explore the impact of physical device dimension, vertical doping profile, and the germanium profile on the origination of transient currents of SiGe HBTs.

2.4.1 Physical Scaling

As SiGe BiCMOS platforms mature, the total active area of the device shrinks. This reduction in area includes shrinking both the emitter window (intrinsic device) and the deep trench enclosure (extrinsic device). The largest impact of this physical scaling is a reduction in the interaction probability of radioactive particles with the active area of a circuit. For an application that is built in an early SiGe BiCMOS generation and ported to a scaled SiGe BiCMOS platform (assuming no changes in architecture), the total sensitive area of the circuit will be reduced. This decrease in sensitive area will manifest itself in a reduction in the frequency of single-events for the application over an identical operational lifetime.

Sutton et al. illustrated this concept experimentally with heavy-ion broadbeam measurements performed on barrel shift registers built with third generation SiGe HBTs [96]. In this study, multiple shift register architectures were fabricated and tested;

one of these registers incorporated minimum sized SiGe HBTs from the process, while a similar register used devices that had a larger emitter window (and correspondingly larger deep trench enclosure). Measurements of the error cross-section curves for these two registers illustrated that there is a significant reduction in the error-cross section across all ion LETs for the minimum-sized shift register. No substantial shifts in the threshold ion LET were measured, indicating that the mechanisms for upset remained identical between the two architectures. The error-cross section curve is a means of expressing the frequency of an error event occurring for a given ion energy and as such supports the argument made in the previous paragraph.

2.4.2 Doping Profiles

In a previous section it was shown the ion-induced shunt results in very large transient currents flowing through multiple terminals of the SiGe HBT. The onset of the ion-induced shunt is strongly dependent on both the ionized free carrier concentration as well as the background doping concentration of the SiGe HBT. It can therefore be expected that the doping profiles will have a substantial impact on the evolution of transient currents for SiGe HBTs. To decouple the impact germanium profile from the doping profile, a standard Si BJT model deck was built from the existing SOI SiGe HBT model deck (by simply removing the germanium in the base). This decoupling is important to isolate any grermanium-induced effects as the metallurgical junctions are modified.

2.4.2.1 Base Doping

To study the impact of base doping on the ion-induced transient terminal currents of a Si BJT, a first-generation, SOI SiGe HBT model was modified to encompass multiple base doping profiles. The five different doping profiles generated, in addition to the control profile for a first generation platform, are shown in Figure 25. Tthe peak base doping was varied between approximately 10^{18} up to 10^{19} cm^{-3}. The decay

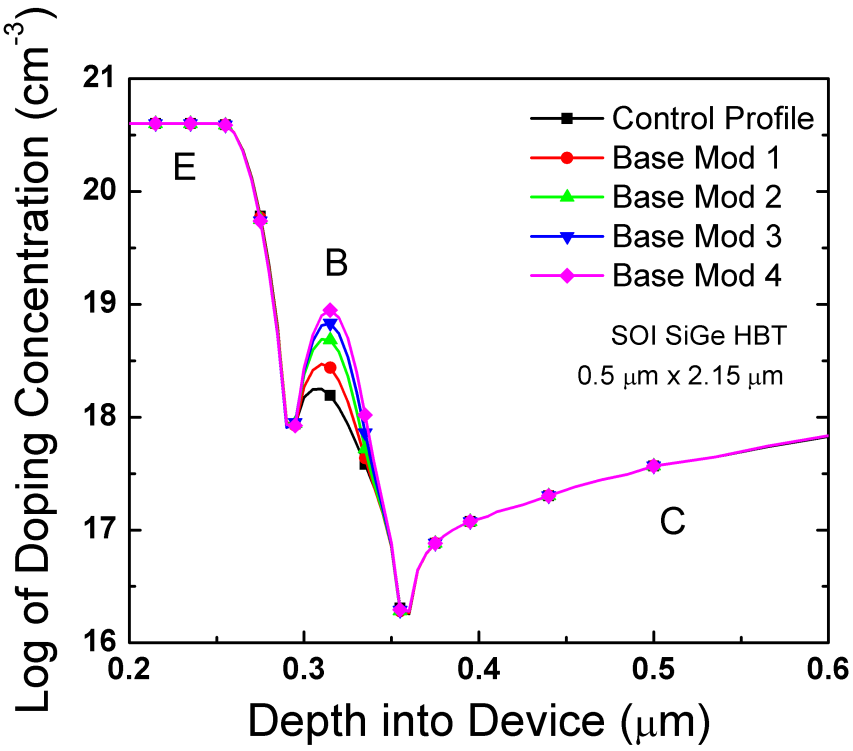


Figure 25: Vertical doping profiles of five *npn* SOI Si BJT variants.

gradients were kept identical such that the metallurgical junction characteristics for the emitter-base junction were not significantly altered. The base doping changes did alter the characteristics of the base-collector junction, shrinking the depletion region with higher peak electric fields. Ion-strike simulations, using an ion LET of MeV-cm^2/mg, were executed for emitter-center strikes on the model decks for all base doping modulations.

The resulting simulated transient current profiles for the collector terminal and the base terminal are shown in Figures 26 and 27, respectively. The emitter current is not shown as it is identical to the collector transient current in its shape, and similar in magnitude. Focusing first on the collector current transients, shifts in both the peak transient amplitude of the waveform as well as the duration of ion-induced shunt current are evident. The changes in the peak magnitude of the transient waveform are tied to the shifts in the gummel curve for each corresponding base doping. The lack

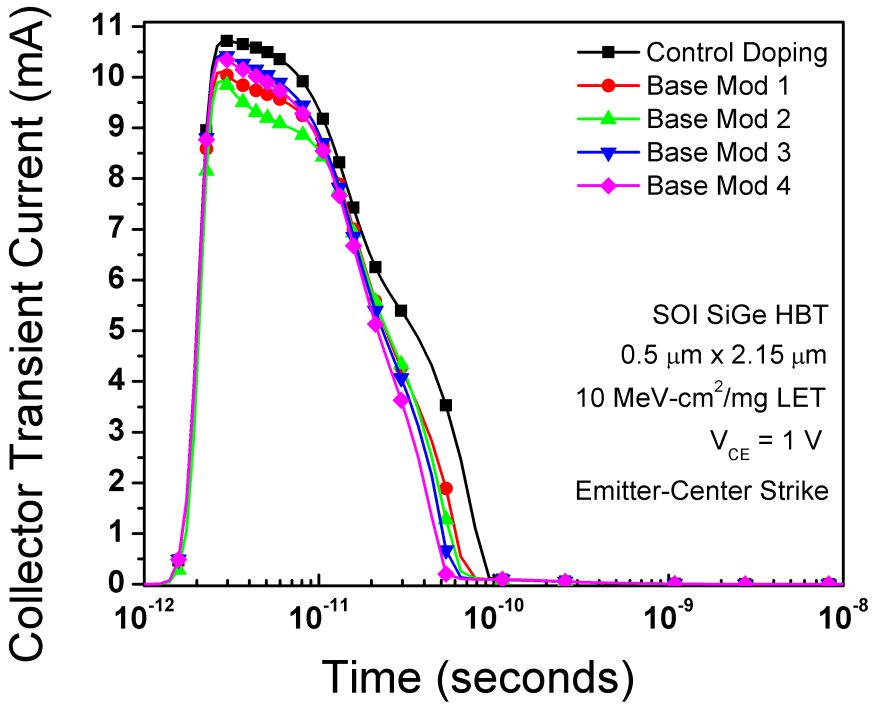


Figure 26: Simulated collector terminal transient currents for multiple base doping profiles of a Si BJT.

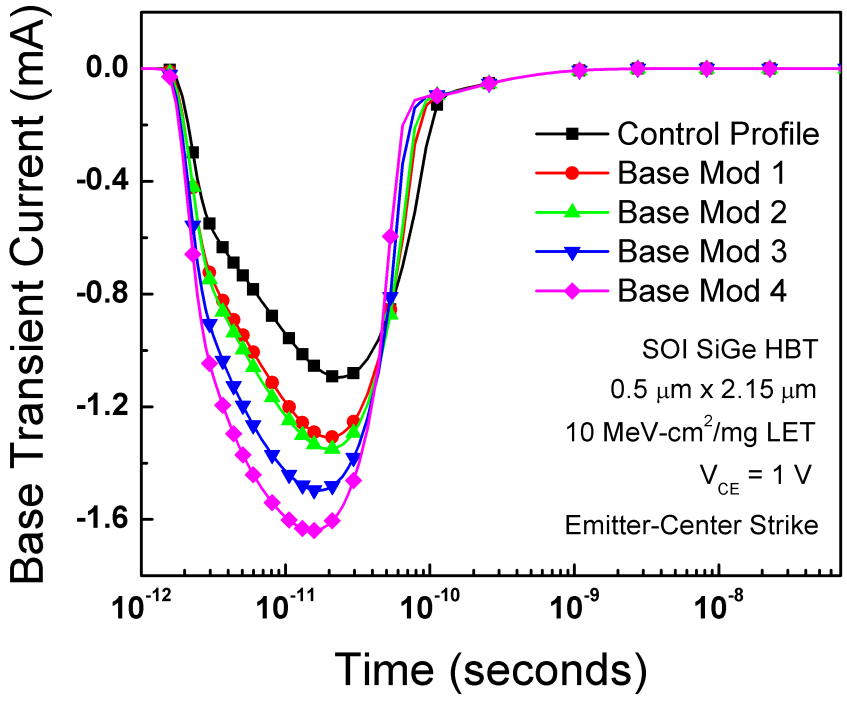


Figure 27: Simulated base terminal transient currents for multiple base doping profiles of a Si BJT.

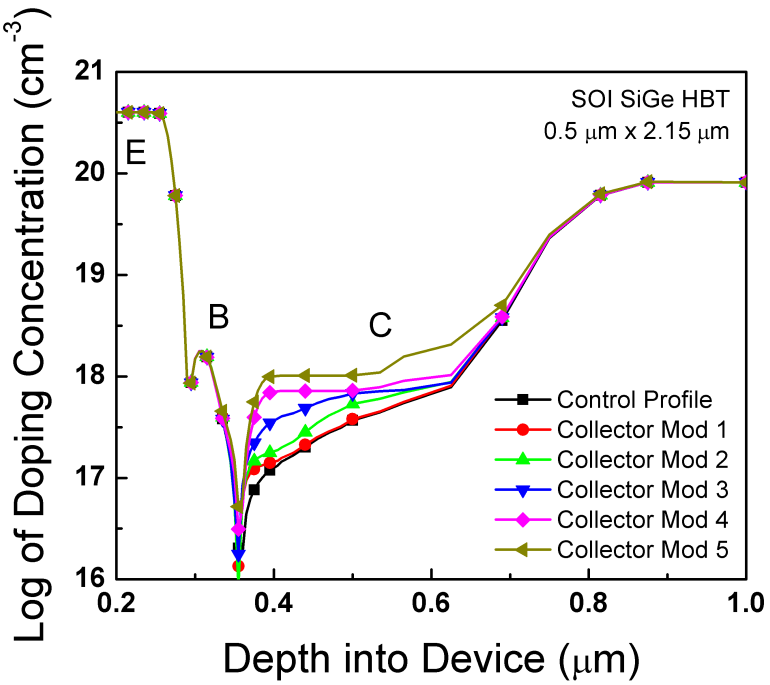


Figure 28: Vertical doping profiles of five *npn* SOI Si BJT variants.

of a trend between the peak transient collector magnitude and the increasing base doping is a result of the dependence of the BJTs collector transfer current on both the base doping and the neutral base width. For the base doping profiles that were generated, the neutral base width was not controlled to be identical between all of the profile variants. This results in the collector transfer current switching between increases and decreases for each step in the base doping. More interesting, however, is the clear trend that exists between base doping and the duration of the ion-induced shunt current. From Figure 26 it is evident that increases in the peak base doping result in steady decreases of the duration of the ion-induced shunt current. With increases to the background doping of the BJT, the duration of the excess ion-induced carrier concentration being larger than this doping is reduced. That base transient terminal current is seen to steadily increase with increasing base doping.

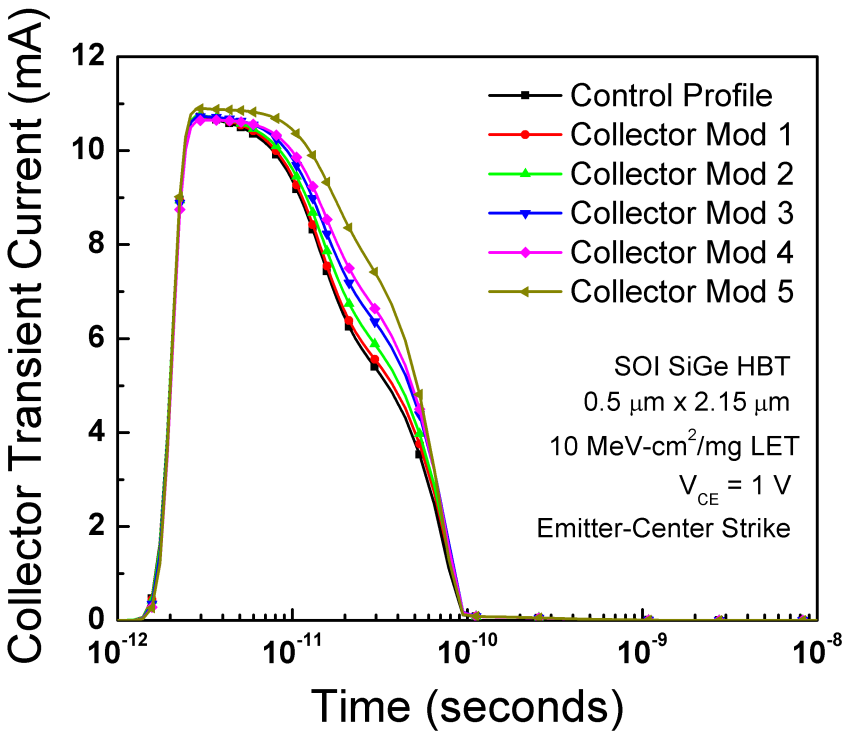


Figure 29: Simulated collector terminal transient currents for multiple collector doping profiles of a Si BJT.

2.4.2.2 Collector Doping

The second doping study probed the impact of the collector profile on the ion-induced transient current waveforms. The collector profile can vary widely between SiGe HBTs within a fixed-generation technology platform [41]. These changes allow the fabrication of tailored device for either high-breakdown or high-performance applications. The five different collector doping profiles generated, in addition to the control profile for a first generation platform, are shown in Figure 28. These variations have a strong impact the collector-base junction, reducing the depletion region width and confining electric field lines. Ion-strike simulations, using an ion LET of 10 MeV-cm^2/mg, were executed for emitter-center strikes on the model decks for all new base doping modulations.

The resulting simulated ion-induced transient current profiles for the collector terminal and the base terminal are shown in Figures 29 and 30, respectively. There are two important features to be taken away from the collector transient currents;

the first is that the peak transient current during the shunt portion of the waveform steadily increases with increasing collector doping. The second point is that there is no change in the duration of the ion-induced shunt with increasing collector doping. The increase in the peak transient current is connected to the electric field distribution in the active region of the device following an ion-strike event. As discussed previously, with the collapse of the collector-base junction, the applied V_{CE} must be supported internally through potential modulation of the neutral regions of the Si BJT. With increasing doping of the collector profile, electric field lines are pushed more into the lower-doped neutral base of the BJT as opposed to the higher-doped collector, resulting in a larger induced forward-bias. This larger distribution of electric field lines in the base results in a greater injection of additional electrons from the emitter, giving rise to a larger transient collector/emitter current. The lack of change in the duration of the ion-induced shunt indicates that the driving mechanism of the shunt effect is the background doping concentration of the lower-doped side of a metallurgical

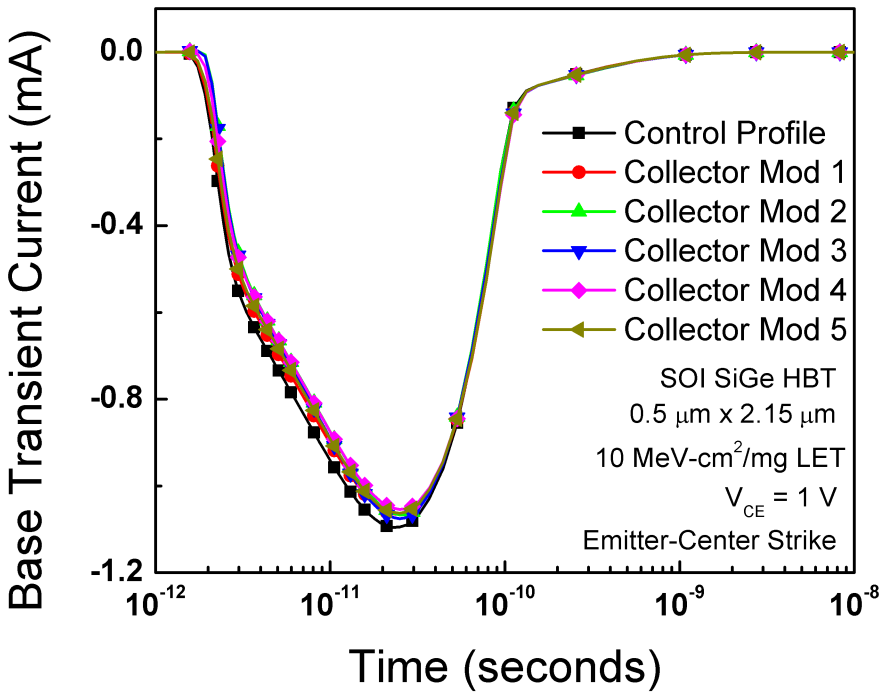


Figure 30: Simulated base terminal transient currents for multiple collector doping profiles of a Si BJT.

junction. The excess carrier concentration must drop below the doping level of the lower-doped side of the junction before the depletion region can be re-established. The base current is seen to remain nearly constant for all variations of the collector profile.

2.4.3 Germanium Profile

In Chapter 1 the influence of the germanium profile of the SiGe HBT on the device physics of the transistor was described. There are multiple implementations of germanium profiles in the base that are employed to achieve different design criteria. Box-like profiles maximize the germanium offset at the base-emitter junction, greatly enhancing the current gain of the HBT. Triangle profiles maximize the germanium gradient in the base of the transistor, giving rise to electric fields that accelerate minority carrier transient and minimize the base transit time. Trapezoidal profiles seek a middle ground between the triangle and the box profile approach, giving both large germanium offsets and germanium gradients in the neutral base. For insight into the impact of germanium profiles on the ion-induced transient currents of the SiGe HBT, four separate SOI SiGe HBT model decks were assembled. The first model deck served as a control, silicon-only BJT, incorporating no germanium in the base. The other three model decks used triangle-shaped germanium profiles, graded over the same physical depth but with varying peaks in the germanium concentration. Triangle profiles were investigated for this study, as the distribution of electric field lines through the base of the SiGe HBT has been seen to play a pivotal role in determining the ion-induced transient current waveforms.

The vertical profile for the devices of these three model decks are shown in Figure 31, where the x-axis is a vertical cut through the emitter-center of the model deck. The germanium profiles were varied between peak mole fractions of 0.1 up to a mole fraction of 0.2, providing three separate distributions of built-in electric field lines through-out the neutral base of the SiGe HBT model. An emitter-center, 10 MeV-cm^2/mg ion

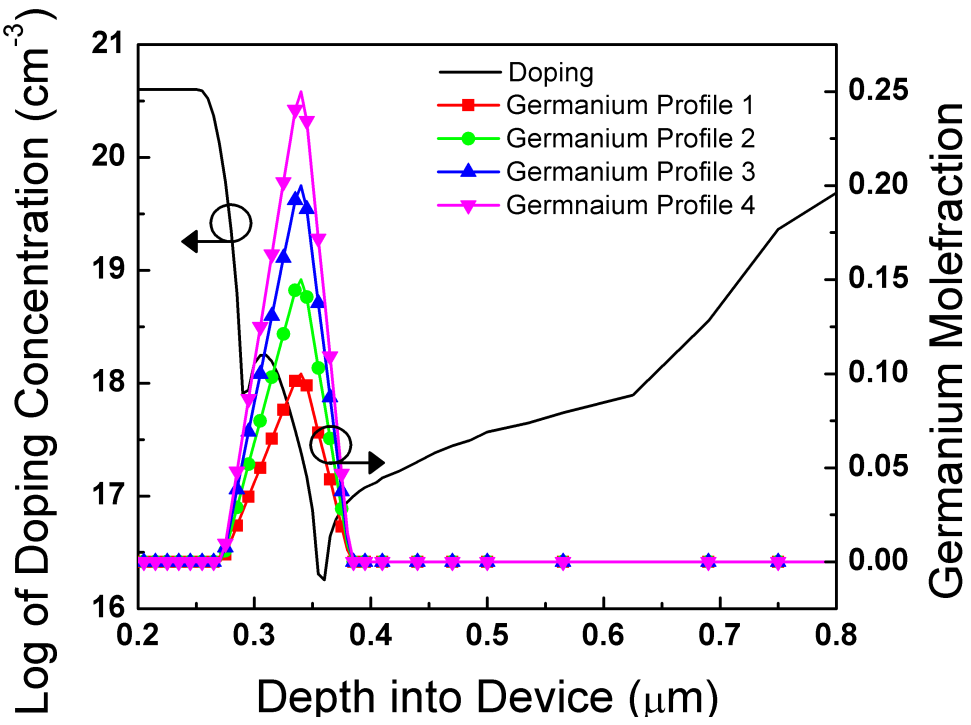


Figure 31: Multiple germanium triangle profiles for a first generation SOI SiGe HBT model.

strike was run for each model deck, with 1 V applied to the collector terminal and 0 V on the emitter and base terminals. The resulting collector transient current for each simulation is plotted in Figure 32. The general shape of the transient current waveform is consistent for all simulations; however, there is a noticeable shift in the peak transient current magnitude which is consistent with the changes in the collector forward transfer current with the germanium profile. It is interesting to see that the variations in germanium grading have little effect on the ion-shunt duration, given the built-in field. One possible explanation for this result is that the control profile is built on a first generation SiGe device profile, which encompasses considerably larger base widths as opposed to higher scaled platforms. With reductions in the base width and identical peak graded germanium mole fractions, the built-in electric field from bandgap narrowing increases. This increase in built-in electric field may have a larger impact on the transient current for third generation profiles as compared to a first

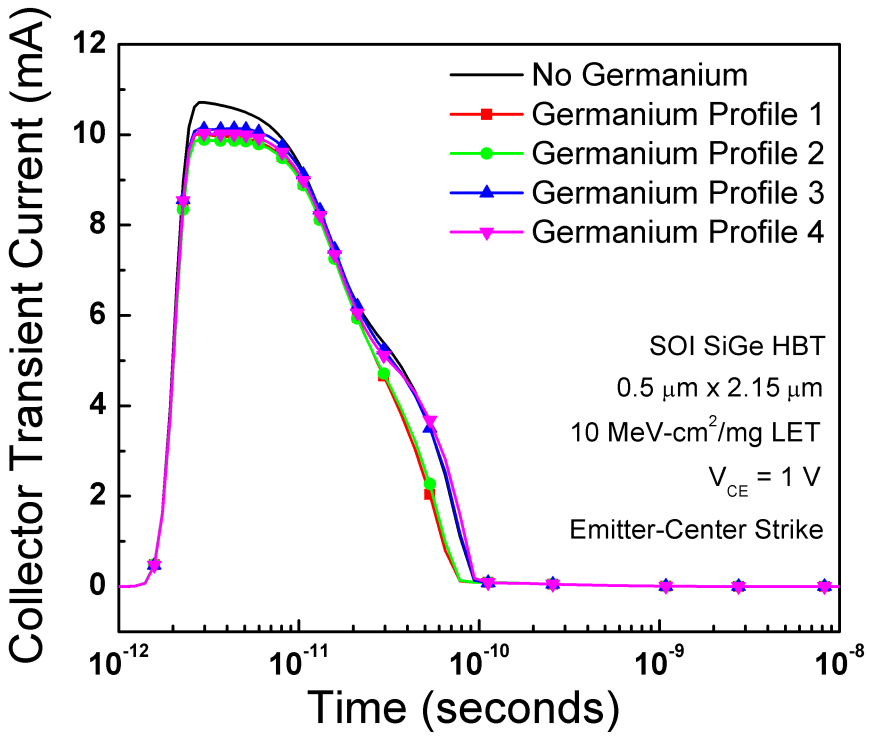


Figure 32: Simulated collector terminal transient currents for multiple germanium profiles of an SOI SiGe HBT.

generation profile.

2.5 Circuit Sensitivity and Radiation Hardening Concepts

This material of this chapter has been dedicated to understanding the physical mechanisms that give rise to ion-induced transient terminal currents of the SiGe HBT and predict the impact of technology scaling on these transient currents. Moving forward, it is logical to next attempt to characterize the impact of these transient currents on the operation of circuits incorporating SiGe HBTs. From this analysis, the sensitive device terminals for a given application can be determined and the necessary steps for improving the radiation tolerance of a system can be outlined. This procedure is not simple, however, and requires extensive simulation for every circuit under investigation, as the impact of transient currents has been shown to be dependent on the bias and loading of SiGe HBT device terminals [72, 109].

Circuit studies of the radiation sensitivity of SiGe HBT systems are rather limited in the literature, as current systems destined for orbital application rely on legacy CMOS hardware. Digital shift registers have formed the framework of SiGe HBT circuit-level investigations as these components are ubiquitous for communication systems. The first heavy-ion broad beam tests of digital shift register circuits fabricated from a first-generation SiGe BiCMOS technology process illustrated some fundamental characteristics of SiGe BiCMOS technology [58]. The first of these characteristics is that circuits built with SiGe technology suffer from a very low threshold-LET. Said another way, SiGe HBTs are very sensitive to relatively small quantities of deposited charge in the context of the active volume of the device. The second characteristic is that the saturated error cross-section of circuits built from bulk SiGe HBTs is very large (on the order of 10^{-3} cm^2). High error cross-sections are indicative of large sensitive volumes that are capable of collecting charge and generating an error event. For SiGe HBTs, the deep trench isolation surrouding the perimeter of the device truncates the lateral sensitive volume, which indicates that the vertical device (specifically the subcollector-substrate junction) is the major contributor of the elevated sensitive

volume.

To gain valuable insight in the dynamics of transient origination and the subsequent generation of error events within a digital master-slave flip-flop, fully coupled mixed-mode simulations have been employed for analysis of a standalone flip-flop built with first-generation SiGe HBTs [68]. From this study, the sensitive mechanisms that give rise to upsets of digital bits within the flip-flop circuit were identified as the ion-induced shunt current and subcollector-substrate funnel current. The ion-shunt current of the SiGe HBT is the limiting limiting factor in deterimning the threshold-LET. This effect is intrisically tied to the vertical stack of the SiGe HBT and is an unavoidable source of sensitivity. The amplification aspect of the shunt-current results in considerable larger quanities of charge induced on device terminals as compared to the actual quantity deposited by an ion within the active area. The second fundamental mechanism driving the generation of errors in a digital flip-flop cell is the transient current originating from the subcollector-substrate funnel that forms for a bulk SiGe HBT. As has been shown in the current chapter, the localized collapse of the subcollector-substrate depletion region results in a push-out of the electric field lines that results charges deep into the substrate being funnled into the subcollector. This mechanism lasts for a considerable duration of time ($\approx$ 1 ns) and as such acts as a primary source of bit upset.

Given the susceptibility of SiGe HBT systems to SEEs, a large amount of research has been dedicated into the development of mitigation techniques to address this sensitivity. The mitigation techniques that have been developed fall within two categories: radiation hardening by process (RHBP) and radiation hardening by design (RHBD). RHBP techniques are the most costly and employ modifications to a standard fabrication flow by either introducing additional mask layers or introducing new materials [21]. Substrate engineering for SEU mitigation is one such RHBP methodology that has been proposed by several organizations and examined through

both simulation and fabricated structures [77, 108, 82]. A commercially available RHBP technique, which considerably reduces the sensitive volume of an HBT, is the replacement of bulk technology with a silicon-on-insulator (SOI) technology [110]. By removing the substrate and using a buried oxide for isolation, the silicon volume where free charge carriers are generated is significantly reduced (standard thinned silicon wafers have substrate thicknesses around 250 - 500 μm compared to $\approx$ 5 - 10 μm epitaxial collector region for SOI processes). More desirable hardening methodologies (from a systems cost standpoint) use RHBD techniques that incorporate device layout or circuit architecture modifications, using a commercial foundry's process as is, with no changes to existing processes or violations of design rules.

The most appealing application of RHBD in SiGe technology is the development of transistor-level modifications that mitigate the introduction of errors from single events. These changes must be compatible with the standard process flow of a technology (no additional mask steps or design rule violations) and not substantially impact the performance of the SiGe HBT. This type of solution would enable the design of standard circuit architectures in radiation environments, eliminating the need for circuit redundancy thereby reducing the power and area overhead required [48]. From the analysis that has been performed in the current chapter, the two primary regions that are targeted for transient mitigation are the ion-induced shunt current and the subcollector-substrate funnel current. Given that the shunt-effect is intimately tied to the inherent vertical stack of the SiGe HBT, device-level RHBD techniques have generally aimed at either mitigating or removing the subcollecter-substrate sensititvity, without resorting to an SOI platform. In the following chapters, several RHBD techniques that have been proposed to tackle this problem are developed and investigated for efficacy.

CHAPTER III

IMPACT OF DEEP TRENCH ISOLATION ON SINGLE EVENT EFFECTS

In the early years of IC fabrication, electrical isolation between transistors on chip was achieved through junction isolation (a reverse biased n+ ring enveloping the device). This isolation tended to have the characteristic of large capacitances between the device collector and substrate as well as large leakage currents under high temperature conditions. Additionally, junction isolation impeded the progress of very large scale integration (VLSI) technology, since large spacing between devices was required. In order to continue the trend of compacting more devices onto a single wafer, a new isolation technique needed to be developed. By etching into the substrate around the device and subsequently filling these trenches with oxide, devices were able to be packed together closer while at the same time reducing parasitic substrate capacitances. This process has become known as deep trench isolation (DTI) [28]. Although previous studies have identified the repercussions of complex charge collection mechanisms in technologies incorporating deep trench isolation [105], no studies have been performed on the potential mitigation of SEE through the inclusion/exclusion of this processing step.

At a preliminary glance, DTI appears to serve a beneficial role in a single event context. As discussed earlier, with the moderately doped substrates in today's SiGe BiCMOS processes, minority carrier diffusion lengths are relatively high. Charges generated deep in the bulk from an ion-generated track are able to diffuse outwards and upwards to the surface. This can easily result in charges being collected by subcollector-substrate junctions of multiple devices, a process known as "charge

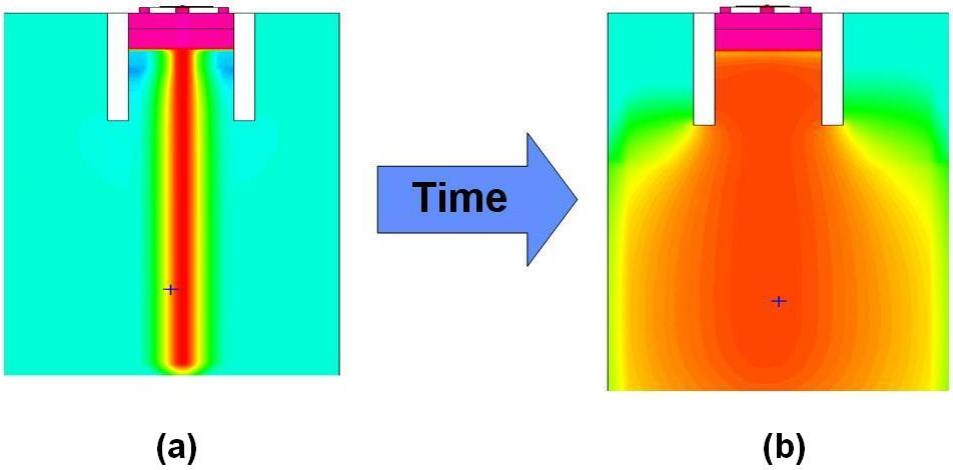


Figure 33: Progression of deposited charge due to an ion strike at times (a) directly after the strike and (b) several microseconds later.

sharing." With the presence of DTI, a significant amount of substrate shielding is introduced, which prevents charge from easily diffusing into the sensitive junctions. Considering an ion strike within the DTI of a device as shown in the cross-sections of Figure 33, the response is more ambiguous and requires investigation.

In Figure 33 the simulated concentration of ionized free carriers as a result of an ion strike to the center of a device is plotted at two given moments in time; (a) directly following the strike and (b) several microseconds after the ion strike. As can be seen, the charge track spreads radially outward to establish equilibrium as well as being "collected" by the subcollector-substrate junction. The DTI is impeding carrier diffusion in the vicinity of the sensitive junction, confining the carriers near the depletion region where they will be collected. This raises the question of whether shallower, or no DTI, would promote more radial diffusion away from the device's sensitive junction, thereby reducing charge collection. To answer this question, devices from two different studies were performed. The first used two, 3rd generation IBM platforms (each having different deep trench depths), which were tested in a heavy-ion microbeam environment to quantify their charge collection statistics. The second

study focused on a single technology platform, where two SiGe HBT were fabricated, one with DTI and one without. Heavy-ion microprobing and heavy-ion broadbeam analysis were performed on these architectures for analysis.

3.1 DTI Depth Dependence

3.1.1 Technologies Under Study

The two platforms used for the DTI depth-dependence study were the 8HP platform [40] (a high performance platform) and the 8WL platform [50] (a cost-effective platform with moderate performance). To distinguish between the two platforms, from here on the 8HP technology will be referred to as the high-performance (HP) platform and the 8WL technology will be referred to as the cost-performance (CP) platform. Both platforms are a 130 nm technology node that share many similar processing steps characteristic of standard high-speed SiGe HBTs. These include a raised-extrinsic base, a retrograded collector, and shallow trench isolation schemes. A cross section of the two platforms is shown in Figure 34. The important difference between the

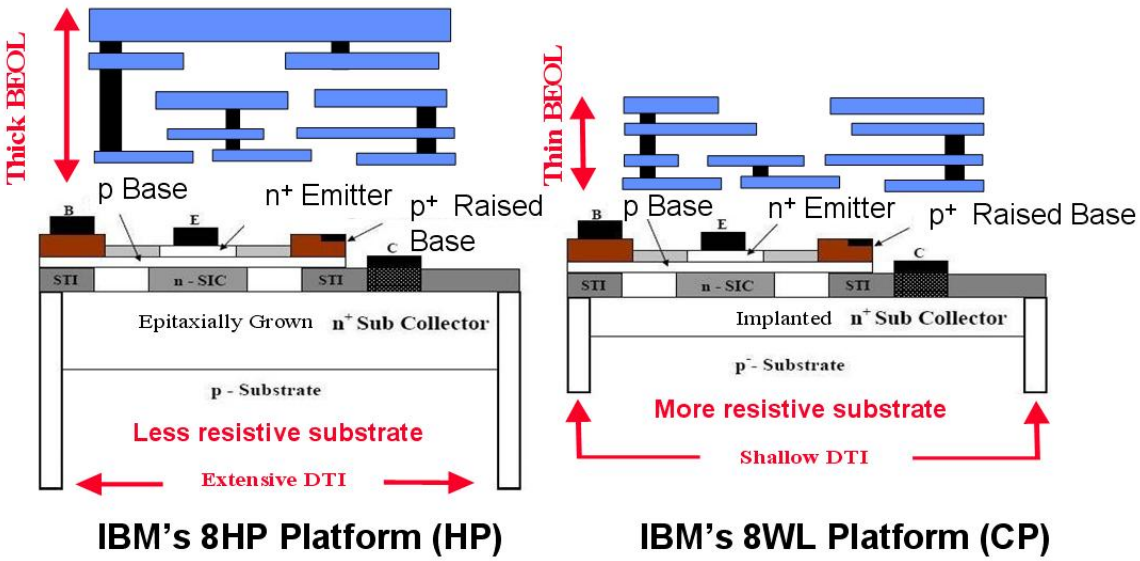


Figure 34: Sample device cross sections for both the HP platform (a) as well as the CP platform (b) are shown, with important process variations, in the context of radiation effects, highlighted.

two platforms, conducive to the experiment at hand, is the depth of the deep trench isolation step. The HP platform uses a trench depth of approximately eight microns while the CP platform uses a trench depth of only approximately 3 μ m.

There are several other differences between the two platforms which need to be accounted for, as they will have an effect on the experiment. These differences include a more resistive substrate, an implanted sub-collector (CP) as opposed to an epitaxially grown sub-collector (HP), different collector reach-through processes, and different back end-of-the-line thicknesses. All of these differences lead to the lower cost of the CP platform.

3.1.2 Heavy-Ion Microprobing

To understand the affects of DTI depth on the SEE susceptibility of the two platforms, a high spatial precision (1 μm x 0.5 μm resolution) heavy-ion microbeam at Sandia National Laboratory's Microprobe facility was utilized to perform charge collection measurements. Identically sized transistors from both the HP and CP deck were irradiated with an ion microbeam, allowing knowledge of the spatial location of the ion strike for a given set of charge collection measurements on the device terminals. All four transistor terminals (base, collector, emitter, and substrate) were monitored simultaneously, with total integrated charge and accompanying X-Y position information recorded for each ion strike event. The experiments were conducted using normally incident 36 MeV ^{16}O ions, having a surface incident linear energy transfer (LET) of 5.4 MeV-cm^2/mg and a range of 25.5 μm in silicon, as determined by the Stopping and Range of Ions in Matter (SRIM) calculations [111]. Samples were prepared in 28 DIP packages with all terminals grounded except for the substrate which was held at negative four volts. These biases were intended to mimic transistor "off-state" conditions, a highly sensitive region of operation for SEU. No etching was performed prior to beam exposure, so any ion energy lost in the overlayers of the devices had to

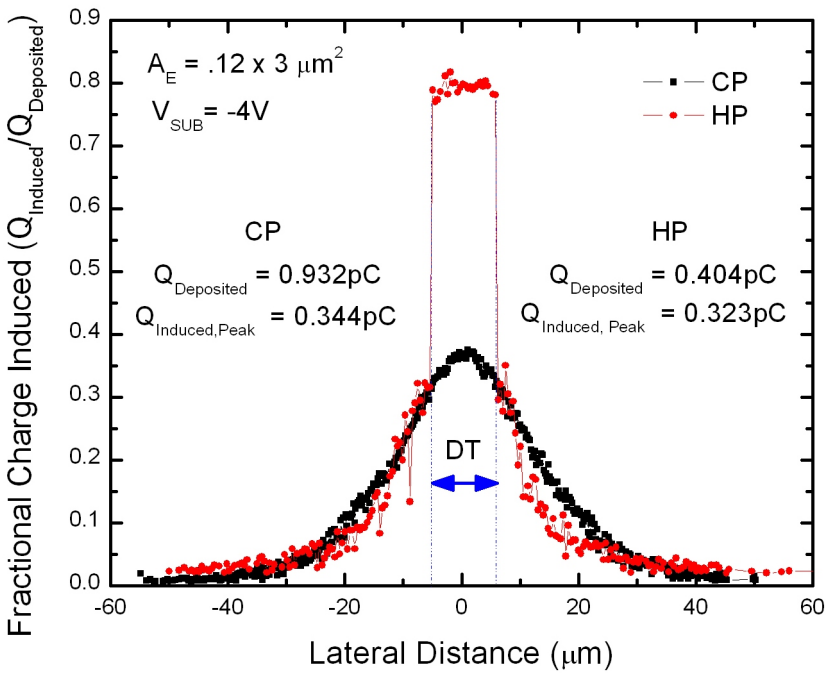


Figure 35: A 2-D cut through the collection peak of the measured fractional collector-collected charge for both the CP and HP devices. Separate charge depositions for the two platforms (due to the substantial BEOL thickness differences) are also indicated, in addition to the peak collection value.

be estimated using SRIM calculations.

IBICC measurements provide three dimensional integrated charge induction profiles for all device terminals. However, given that current-mode digital bipolar logic (CML) typically employs the collector node of the transistor as the output node of the circuit, we focus on the collector-induced charge following an ion strike. Figure 35 shows two dimensional cuts through the center of the devices of the three dimensional collector-induced charge data sets (Z direction collapsed onto the X-Y plane with one coordinate held constant) obtained for both the CP and HP SiGe HBTs.

The data has been plotted in the form of a fractional charge induced ($Q_{induced}/Q_{deposited}$) since ion energy loss in the overlayers of the devices are not equivalent, implying different amounts of charge deposited in the two platforms. As mentioned previously, the HP platform has a distinctly larger BEOL process due to both increased number of metal layers and thicker metal layers. Back calculating the energy lost of the oxygen

ion in these overlayers using SRIM, we find that there are significant differences in the energy of the oxygen ion penetrating the surface of each device. These differences in energy will correspond to two distinct LETs for the ions striking the two platforms, hence two separate amounts of deposited charge. For the CP platform, the 36 MeV oxygen ion is attenuated to 29 MeV, or a corresponding LET of 5.69 MeV-cm^2/mg, while for the HP platform the oxygen ion is attenuated to 9 MeV, or an LET of 6.93 MeV-cm^2/mg. The theoretical charge deposited, calculated from the ion LET and penetration depth, is 0.932 pC and 0.404 pC for the CP and HP platforms respectively.

By plotting the fractional induced charge, the response to an ion strike is normalized, and the two platforms can be directly compared. There are several striking characteristics to be noted from Figure 35, the first being that the shallower trench isolation ($\approx 3\mu m$ for CP as opposed to $\approx 8\mu m$ for HP) of the CP device leads to an increase in collected charge outside of the subcollector-substrate junction (defined by the boundaries of the trench isolation). As opposed to the sharp drop in induced charge for HP devices due to deep trench isolation (trench boundaries indicated by arrows in Figure 35), deposited charges in the CP device outside of the active area can freely diffuse towards the subcollector-substrate junction and be collected. This gradual, smooth decrease of induced charge on the collector terminal moving outwards from the active area of the CP device implies a wider range of sensitive area for upsets when compared to the HP device. Full 3-D TCAD simulations of ion strikes in these two platforms complement this measured data and provides insight into the physical mechanisms driving the results.

3.1.3 3D TCAD Modeling

Full three dimensional models of devices from both platforms were built using Computational Fluid Dynamics Research Corporation's (CFDRC) finite element modeling

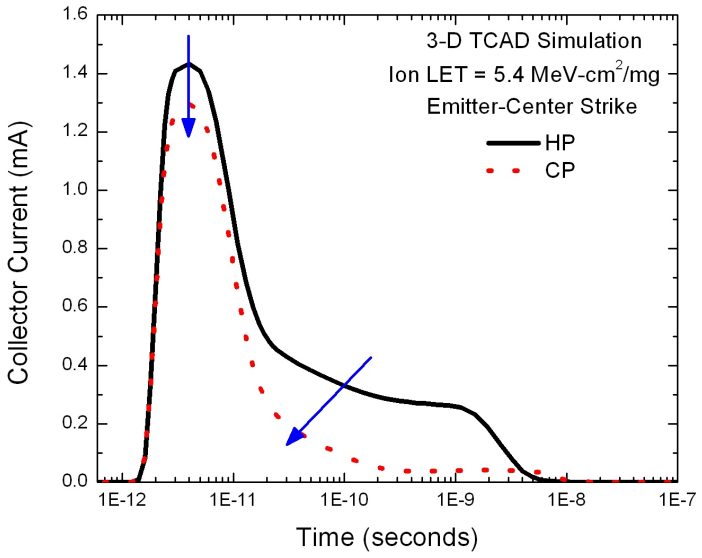


Figure 36: Induced collector current transients from an ion strike normal to the emitter with an LET of 5.4 MeV-cm^2/mg. Reductions to peak current and significant mitigations of "tail" currents are evident for the CP device.

software package NanoTCAD. The decks were calibrated to both measured dc characteristics, as well as microbeam data; an iterative process involving adjustment of minority carrier lifetime model parameters within various semiconductor regions. NanoTCAD ion strike simulations employ a Gaussian charge generation with a peak time of two picoseconds. An ion LET of 5.4 MeV-cm^2/mg was used for both platforms for a direct comparison of the charge collection mechanisms inherent to each platform. The spatial location for the ion strike was initially chosen to be the center of the emitter for both the CP and the HP device. This position has been determined to be the most sensitive strike coordinate from Chapter 2, resulting in an ion passing through all junctions of the device. Figure 36 shows the current transient waveforms acquired from the simulation of a normally incident ion strike on the center of the emitter of both devices.

These waveforms retain a similar shape between the two platforms; a shape that has been attributed to quick collection of charges from modulated electric fields in the substrate (the classic funnel effect), coupled with drift-diffusion collection of generated

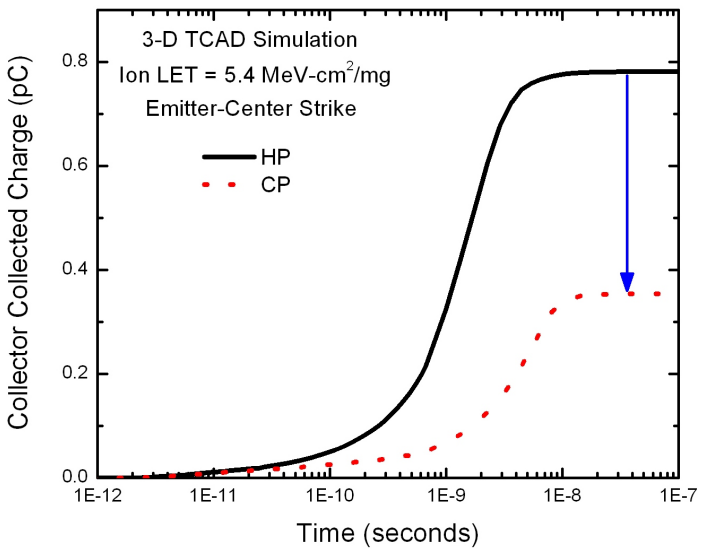


Figure 37: Integrated collector-collected charge for simulated emitter-center ion strikes to identical area (0.12 μ m x 3 μ m) CP and HP SiGe HBTs. A near 50% reduction in collected charge is observed for the CP device.

carriers [26, 27, 61, 20]. There is significant attenuation of the slow tail collection (20 ps to 20 ns) in addition to a lower, maximum peak current spike in the transient for the CP platform when compared to the HP platform. This current reduction couples to a reduction in the total integrated charge which is induced on the collector terminal, as seen in Figure 37.

While the simulated charge collection of the HP platform due to an ion strike with an LET of 5.4 MeV-cm^2/mg is approximately 0.8 pC, the CP platform only collects approximately 0.35 pC for an ion with equivalent LET. This is a substantial decrease in the charge collected at the collector terminal, and to understand the large difference between these two charge collection profiles, the time evolution of the drift and diffusion current components of the generated charge is examined. These current profiles are taken along a two dimensional cut at specific z-locations (depth of the device). Figure 38 and Figure 39 show the time evolution of the electron drift current density projected on the X-Y plane with one spatial coordinate held constant for both technology platforms. The location of the Z-cut was identical for both the CP and

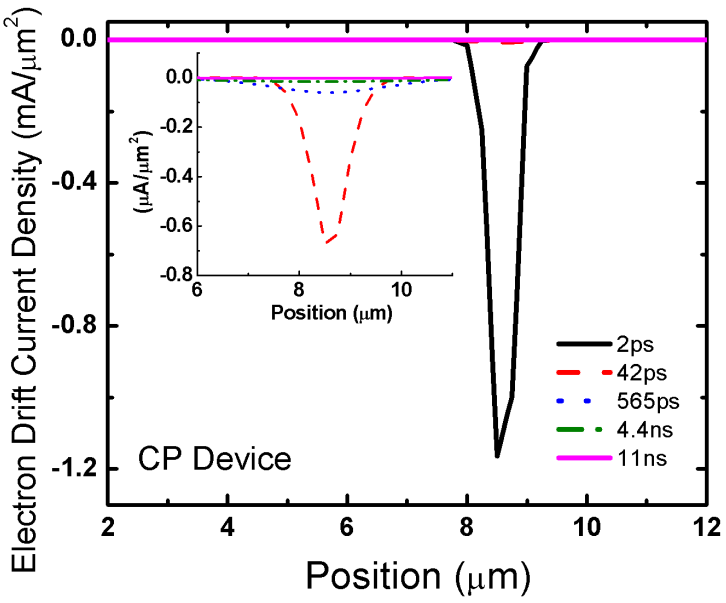


Figure 38: Time evolution of the electron drift current density of the CP device in the Z-direction, collapsed on the X-Y plane and plotted with one spatial coordinate held constant. The inset shows a magnified plot of the drift current density μ A/μ m^2) for times well beyond 2 ps. The electron drift component quickly falls off to extremely low values after only 42 ps following the strike.

HP platforms and was located directly below the bottom of the deep trench of the HP device.

The drift component is observed to be consistently higher for the HP device, stemming from larger field perturbations in the substrate which accelerate electrons in the charge track up into the subcollector-substrate depletion region. Although the CP device also shows a large drift contribution early after the strike (2 ps), the term is smaller than in the HP case, and quickly shrinks in magnitude. This smaller drift contribution is attributed to the CP platform's lower peak transient collector current. To understand the origin of this smaller drift current, it is hypothesized that the presence of the deep trenches in the HP platform impedes carrier diffusion away from the sensitive junction; confining free carrier within the trench boundaries and resulting in them being collected across the depletion region. To verify this claim, the diffusion of the carrier concentration over time was analyzed for both simulated device

decks.

To understand the rapid drop in the electron drift current component in the CP device, the projection of the time evolution of the radial distribution of generated charge carriers on the X-Y plane is plotted in Figure 40 and Figure 41, for the CP and HP platforms, respectively. The location of the Z-cut was once again identical for the two platforms and was located directly below the bottom on the deep trench of the HP device. The data from these simulations support the earlier hypothesis that the presence of deep trenches impedes the radial dispersion of free carriers (even below the deep trench!) causing elevated charge collection values. Immediately following the strike, both platforms have nearly the exact same carrier concentration distribution within the charge track. Given that the peak carrier density in the charge track remains roughly constant between the two platforms, yet drift currents are not equivalent, larger carrier diffusion components are expected to be noticeable in the CP device.

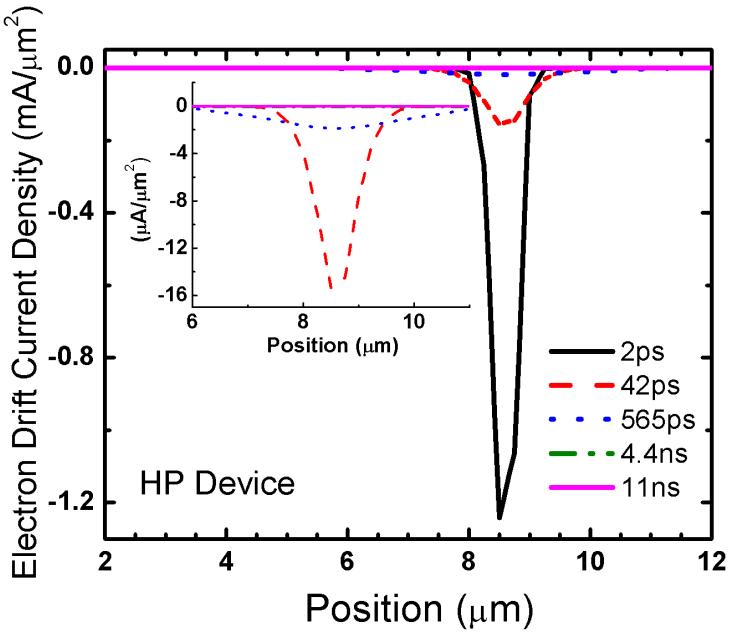


Figure 39: Time evolution of the electron drift current density of the HP device in the Z-direction, collapsed on the X-Y plane and plotted with one spatial coordinate held constant. The inset shows a magnified plot of the drift current density (μ A/μ m^2) for times well beyond 2 ps. The electron drift component maintains distinctly non-zero values for nearly a nanosecond after the strike.

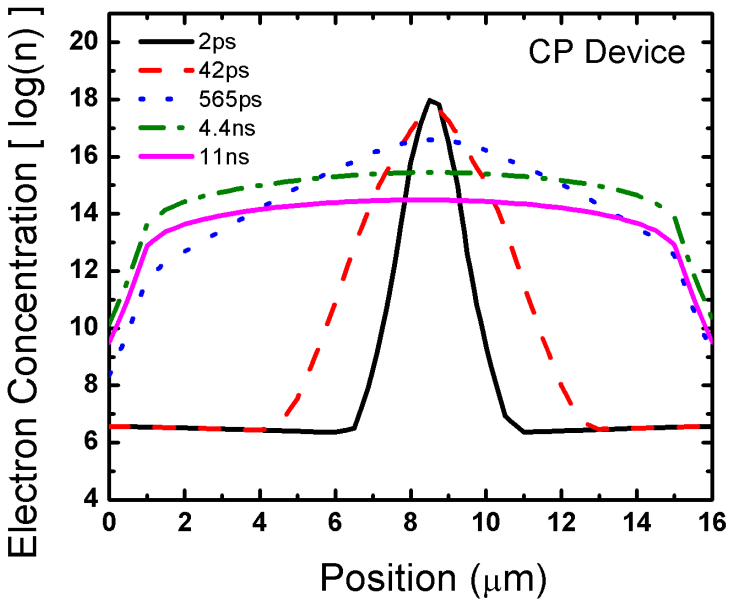


Figure 40: Time evolution of the radial diffusion of the carrier concentration of the CP device in the Z-direction, collapsed on the X-Y plane and plotted with one spatial coordinate held constant. Large diffusion is evident with smooth spreading of the peak spatially outward in both directions.

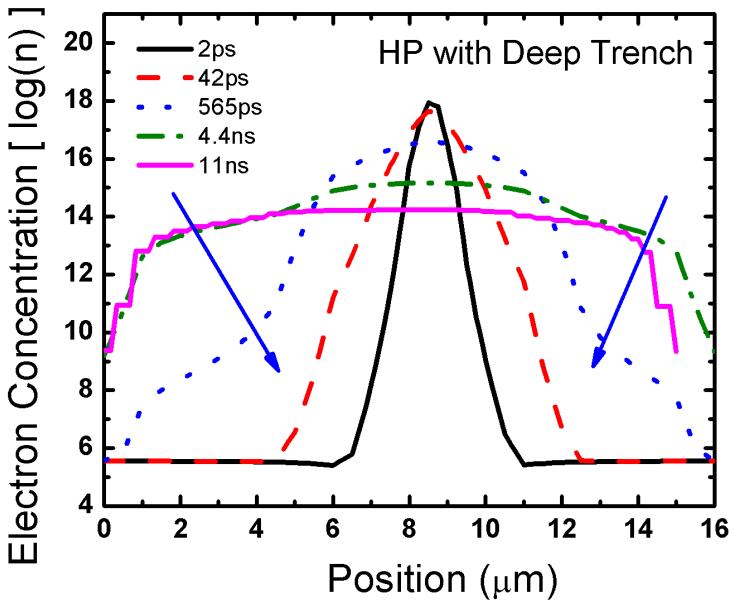


Figure 41: Time evolution of the radial diffusion of the carrier concentration of the HP device in the Z-direction, collapsed on the X-Y plane and plotted with one spatial coordinate held constant. Significant variation in diffusion between the CP is evident for tims greater than 565 ps.

Increased radial diffusion of free charges is evident in the CP device, with smooth reductions in the peak as carriers spread outward into the quasi-neutral substrate. Referring to Figure 41, the HP device clearly shows slower radial diffusion of charge carriers, even for charges below the deep trench implying a coupling effect between charges confined within the DTI, to the charges in the track below the DTI. Significant difference between the diffusion of the two platforms is especially noticeable for a time of 565 ps after the ion strike. Although the peak carrier concentration remains relatively similar between the two devices at this time, distributions spreading from the peak are quite different. Given that charge deposition is identical between the two platforms and there is a similar peak concentration for both devices, the charge that has not diffused in the HP device has drifted to the sensitive junction and been collected. With limited differences between technologies, the factors which could impact the charge collection process for the two platforms are the substrate resistivity and the DTI. Previous substrate resistivity studies have shown that higher resistive substrates should suffer from larger charge collection events [72] (in contrast to the measured data and simulations performed herein); therefore, we attribute the decreased sensitivity of the CP device to variations in the depth of the deep trench isolation.

3.2 DTI Removal

To complete the study of the dependence of deep trench isolation on ion-induced transient terminal current origination and subsequent error propagation, a new set of custom-designed 8HP hardware was fabricated with the deep trench processing step completely removed from the device structure. This process modification did not impact the transfer characteristics of the device. A digital shift register, constructed from SiGe HBTs with no DTI, was fabricated to explore the measured SEU impact of eliminated the external isolation. Finally, a new, calibrated 3D TCAD model deck was also assembled to model this new device structure. The analysis begins with a

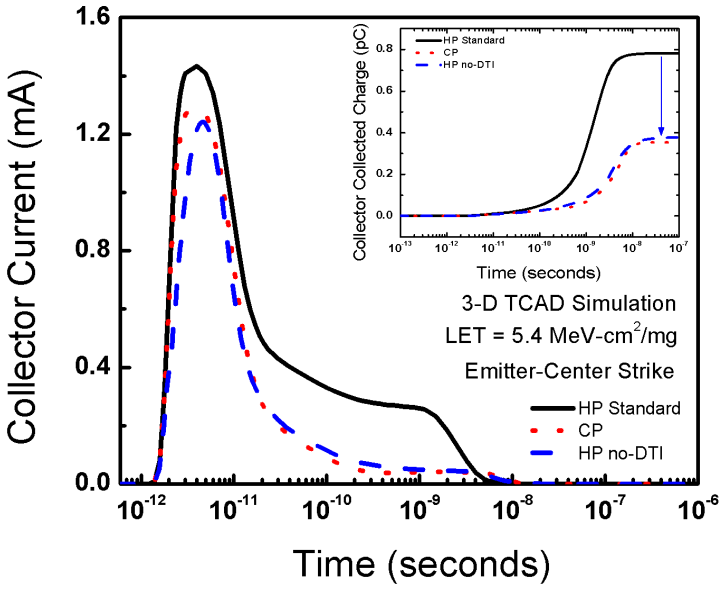


Figure 42: Induced collector current transients plotted for all three device decks. Very similar behavior observed between the HP with no DTI deck and the CP deck.

discussion of the 3D TCAD results and continues to conclude with the heavy-ion broadbeam data on the digital shift registers.

3.2.1 3D TCAD Modeling

For a direct comparison of trench dependence on charge collection events, an additional TCAD model deck was constructed using the model parameters from the HP device. This variant incorporated all of the features of the HP platform, except complete elimination of the DTI. No variation in substrate resistivity was made between these two model decks. An ion LET of 5.4 MeV-cm^2/mg was used for all strike simulations. A plot of the current transient waveforms acquired from the simulation of a normally incident ion strike on the center of the emitter of both the DTI and no-DTI device is shown in Figure 42.

Strong similarities between these results and those for the CP/HP comparison are evident; namely a reduction in peak transient current as well as attenuation of the current tail which couples to a reduction in total charge collected. Examination of the time duration of electric field lines penetrating into the substrate show an equivalent

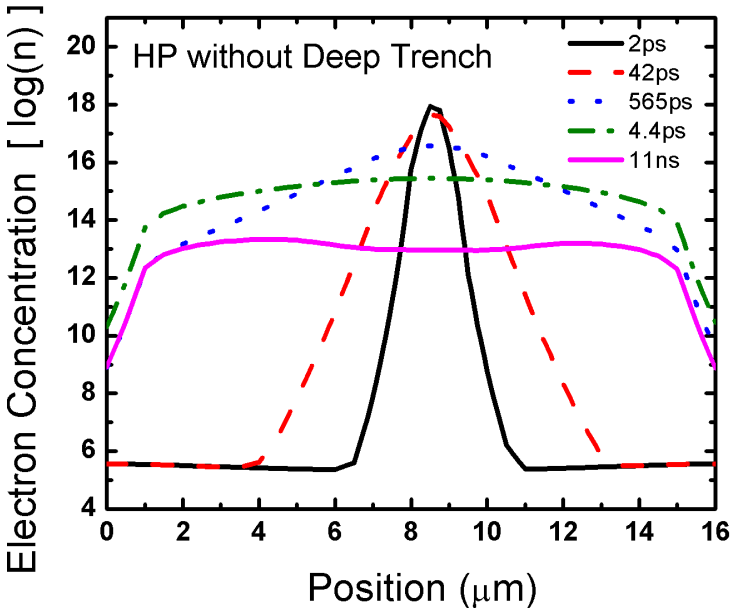


Figure 43: Time evolution of the radial diffusion of the carrier concentration of the HP with no DTI device in the Z-direction, collapsed on the X-Y plane and plotted with one spatial coordinate held constant. Similar to the CP platform, much larger diffusion arises when compared to the standard HP device.

period of charge funneling (which is expected given the identical substrate resistivity); however, smaller electron drift currents exist for the no-DTI device. Once again this reduction can be attributed to larger radial diffusion of charge carriers from the charge track. The projection of the time evolution of carrier density on the X-Y plane is plotted at a depth corresponding to the bottom of the deep trench in DTI device in Figure 41 and Figure 43, for the DTI device and the no-DTI device respectively.

Similar again to the CP device, the no-DTI structure exhibits faster spreading of free carriers from the center of the charge track, generating large diffusion away from the sensitive junction where charge would be collected. This implies that charge collection differences between the HP and CP platform can be attributed to the depths of the deep trench. For emitter-center strikes, it has been shown that charge collection decreases as the depth of the DTI is minimized, peaking when there is absolutely no trench isolation. Previously we have mentioned that DTI does serve a purpose in shielding ion strike events occurring outside the active area of the device; therefore, it

is necessary to analyze the impact of reduced trench depths for these strike locations.

Up to this point, only simulated ion strikes orthogonally incident (i.e. vertical strikes) on the emitter of a device have been under consideration. Despite being the most efficient volume for charge collection events, sensitivity to SEU also exists for ion strikes occurring in the exterior of the trench-enclosed volume, as well as for angled strikes. Recalling the large minority carrier diffusion length of charges in the bulk of SiGe technologies, charges deposited well outside the DTI boundary will have a high probability of diffusing to the active area of the device and be collected before undergoing recombination events. Space is a broadbeam environment and the exact spatial location of an ion strike can not be predicted; however, comparing the ratio of interior trench area to the area outside DTI, there is a much higher probability for strikes outside the trench. For many SiGe processes, the sensitivity to outside DTI is much less than that for normal emitter-center strikes because of the impedance to carrier diffusion due to deep trench isolation; however, critical charge values for upset have been found to be as low as 100 fC; a quantity which could be collected after outside-DTI strikes for large values of ion LET [87]. For structures which have eliminated or shallower DTI, this sensitivity is greatly enhanced.

The induced collector current transient waveforms as well as integrated charge for the CP device, standard HP device, and no-DTI HP device are shown in Figure 44 for an ion with an LET of 5.4 MeV-cm^2/mg striking 1 μ m from the DTI boundary. Both the CP platform and the HP device with no DTI show greatly enhanced collector current transients, coupling to much larger integrated charges; however, the no-DTI device shows a distinctly different current waveform shape from the other devices. This variation, having much larger currents, is due to the partial collapse of the subcollector-substrate junction from free carriers flooding the depletion region. With no trench isolation impeding the diffusion of carriers to the active area, charges can freely move into the depletion region and compensate the fixed charges present,

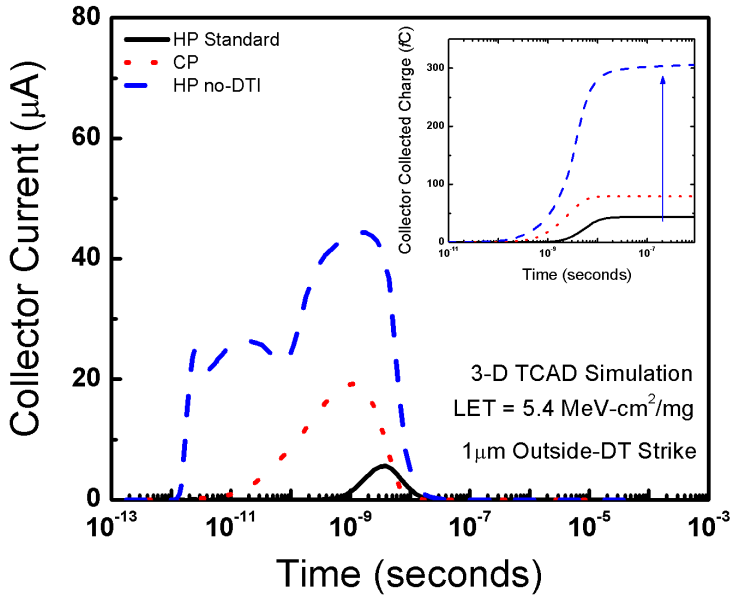


Figure 44: Induced collector current transients from an ion strike normal to the emitter with an LET of 5.4 MeV-cm^2/mg with an inset showing integrated charge collected. Increases in collected charge for outside DTI strikes are observed for devices with limited DTI and extreme increases are seen in the no-DTI.

collapsing the space charge region. The collapse in the depletion region will result in electric fields being pushed into the substrate to support the applied reverse bias to the subcollector-substrate junction, accelerating charge collection through the funneling mechanism.

3.2.2 Heavy-Ion Probing

To experimentally explore the impact of eliminating the DTI from the SiGe HBT device architecture, custom 3rd generation SiGe HBTs from IBM's 8HP technology process that excluded this isolation layer were fabricated. These devices were packaged on high-speed PCB boards with all device terminals connected to independent SMA launchers, such that TRIBICC testing could be performed at Sandia National Lab. A set of control devices (nominal 8HP SiGe HBTs of matched emitter area that included the DTI) were also packaged for TRIBICC purposs for comparison purposes. The 36 MeV ^{16}O ion beam was rastered across both SiGe HBTs to probe the senstive area

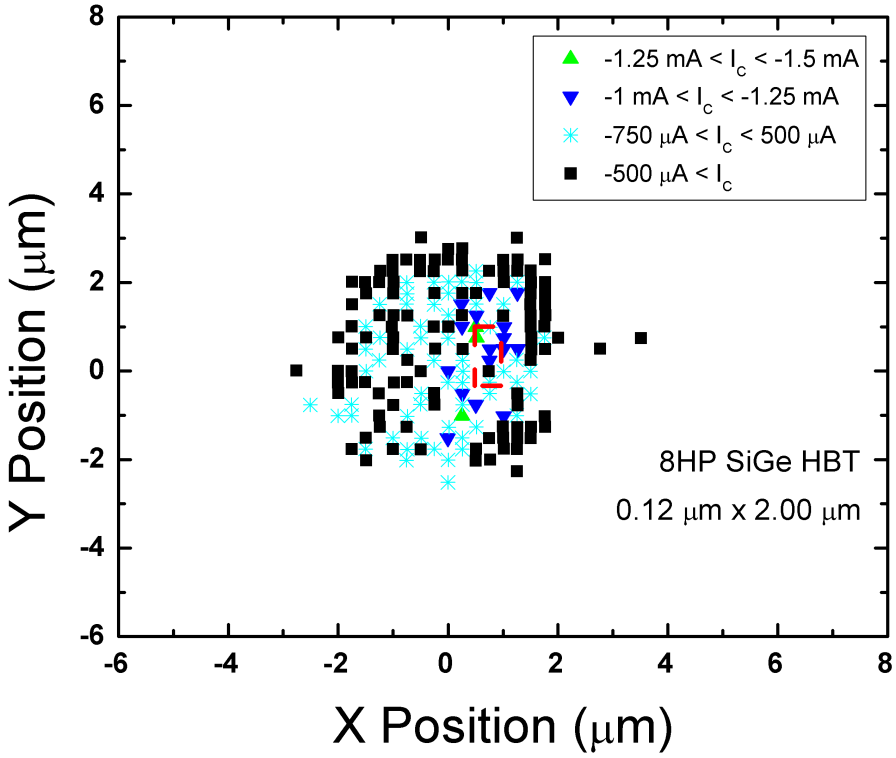


Figure 45: Peak collector transient current of a standard 8HP SiGe HBT, plotted as a function of the spatial location of the ^{16}O ion beam.

of the structures. From the transient data collected, 2-D maps of the sensitive area can be assembled by plotting the magnitude of the peak transient current for any device terminal on an X-Y coordinate plane at a position corresponds with the strike location of the ion beam. The peak collector current transient magnitude maps for the standard 8HP SiGe HBT and the no-DTI 8HP SiGe HBT are plotted in Figure 45 and Figure 46, respectively.

The emitter area for both transient maps is outlined with a red-dashed box, to provide a reference position for the location of transient events. Clearly the measured sensitive area for the no-DTI structure is considerably larger than sensitive area of the standard SiGe HBT, a result that supports the previous 3D TCAD simulations of no-DTI structures. The increase in the sensitive area resulting from the elimination of the DTI is linked to two phenomena: (1) an enhancement of charge diffusion for ion strikes occuring far from the active area of the device, a result which was illustrated in

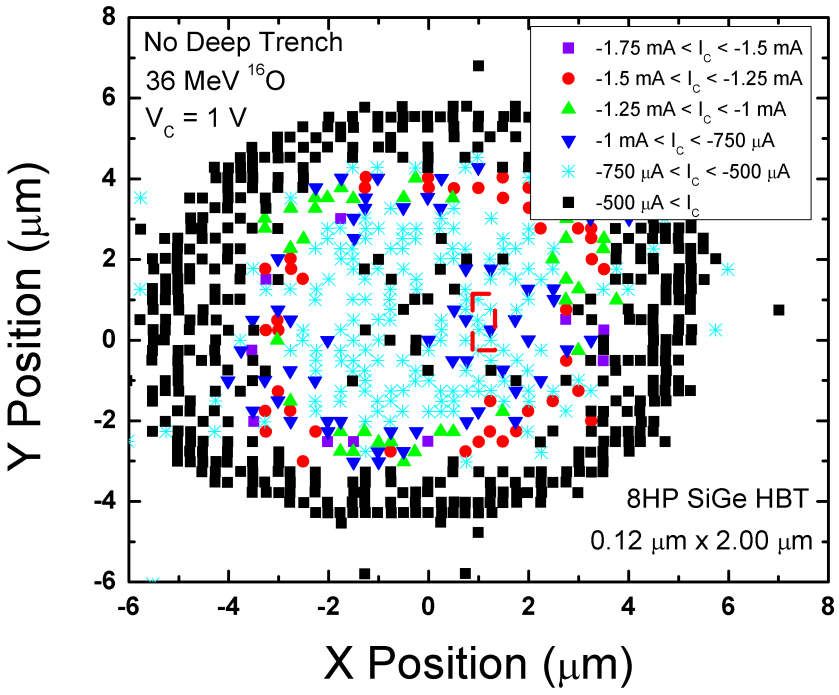


Figure 46: Peak collector transient current of an 8HP SiGe HBT with no DTI, plotted as a function of the spatial location of the ^{16}O ion beam.

the TCAD simulations, and (2) the presence of a lateral depletion region that forms between the implanted subcollector and the substrate. The presence of the lateral depletion region is evident in the transient map from the ring of high-peak transient currents that surround the active-area of the HBT. The combination of a vertical and lateral depletion region creates a large volume of silicon with electric-field lines that can collect deposited charge from the ion-strike, generating much larger transient currents as compared to an ion-strike passing only through the vertical subcollector-substrate depletion region. Although there is a substantial increase in the sensitive area of the no-DTI SiGe HBT, a comparison of emitter-center collector and substrate transient currents for a standard device and a no-DTI device, shown in Figure 47, reveals that the elimination of the DTI reduces the duration of the transient current induced on the collector and substrate terminals. This TRIBICC result complements the preliminary IBICC data and the subsequent 3D TCAD simulations that illustrated a reduction in terminal transient current as a result of improved ambipolar diffusion away from the

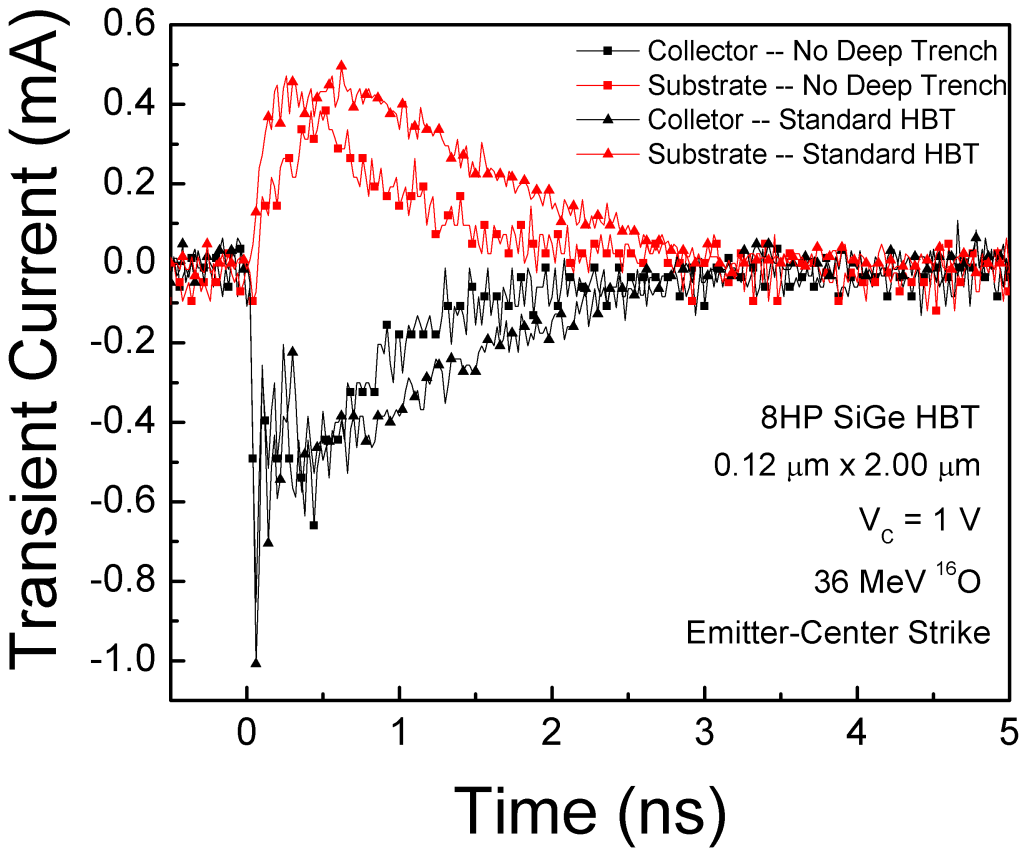


Figure 47: A comparion of measured, ion-induced collector and substrate terminal transient currents induced on an 8HP SiGe HBT both with DTI and without DT.

sensitive depletion regions of the SiGe HBT. The cost of the extension of the sensitive area of the no-DTI would appear to outweigh the minor gains in the reduciton of the active-areas strikes.

To verify the previous claim two 16-bit digital shift register architectures, assembled using the triple-tail cell latch architecture, were fabricated [43]. The first variant incorporated standard 1st generation SiGe HBTs while the second variant had 1st generation SiGe HBT without DTI. Both architectures were fabricated with IBM's 5AM SiGe BiCMOS technology process. These structures were packaged and tested at the Texas A&M Cyclontron Institute using multiple heavy-ion broadbeams to cover a large spectrum of space-relevant LET values. The caluclated error cross-curves for both shift register architectures are plotted in Figure 3.2.2. While both shift registers

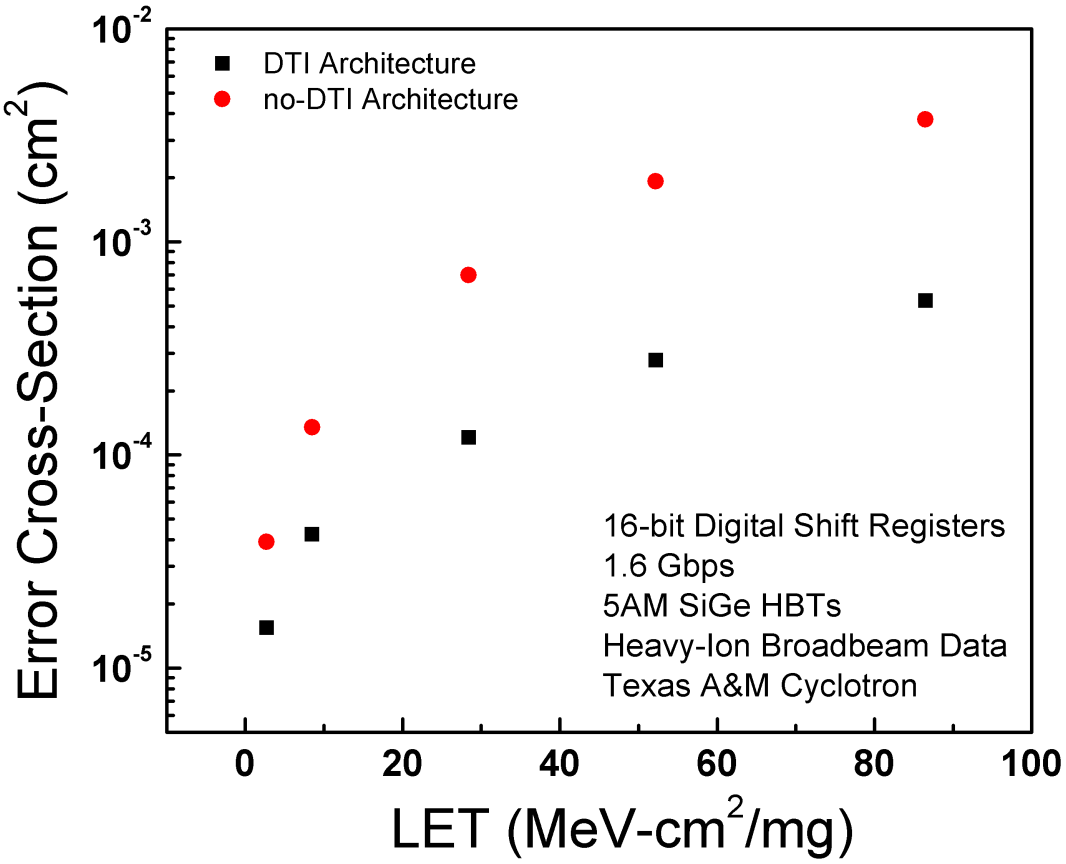


Figure 48: A comparion of measured error cross-section curves for two 16-bit shift registers structures, one constructed with standard 1st generation SiGe HBTs, the second with 1st generation SiGe HBTs with no DTI.

exibit identical threshold-LETs, the saturated error cross-section for the no-DTI shift register is considerably larger than the variant incorporating standard SiGe HBTs. This difference is linked to the increase in the sensitive area of the no-DTI HBT arising from the presence of the lateral subcollector-substrate depletion that forms from the removal of the DTI. The elevated error cross-section will lead to significant degradation in the bit-error rate performance of a system constructed from no-DTI devices, which precludes its application in radiation environments.

3.3 Conclusions

I have demonstrated, both with experimental data and calibrated 3D TCAD simulations that the presence of the DTI of a SiGe HBT is intimately tied to the origination

of ion-induced transient terminal currents. The DTI acts as a confining boundary for charges deposited vertically through the device structure, preventing ambipolar diffusion away from the sensitive subcollector-substrate depletion region. The reduction of the DTI layer was experimentally shown to give a reduction in the collected charge (and subsequently the transient current amplitude and duration) for ion-strikes through the active area of a SiGe HBT at the expense of extension of sensitivity exterior to the deep trench boundary. Complete removal of the DTI was found to also mitigate transient origination for active-area strikes; however, the formation of a lateral depletion region of the subcollector-substrate junction around the device perimeter significantly extends the sensitive area of the device. This extension results in considerable increases to error counts of digital circuits built with no-DTI HBTs; therefore, the optimal solution is a minimum-depth deep trench (extending to the depth of the subcollector implant) to prevent the formation of a lateral depletion region while maximizing the ambipolar diffusion of deposited carriers. The outsanding issue of mitigating transient events from ion-strike external to the deep trench still remains, however.

A proposed method for almost completely mitigating charge collection outside of the DTI of a SiGe HBT is the N-Ring SiGe HBT [96, 106]. With the incorporation of a highly doped n+ diffusion layer encompassing the device, a shunt path for minority carrier electrons is introduced, which reduces carrier concentrations reaching the sensitive subcollector-substrate junction. Incorporating these structures into platforms with limited to no DTI (essentially reverting back to a junction isolation platform) could eliminate the caveat of exaggerated charge collection of outside-DTI strikes while maintaining reduced collection for ion strikes in the active areas of the device. The investigation of the impact of N-Rings in SiGe HBTs is presented in the next chapter.

CHAPTER IV

N-RING SIGE HBTS

4.1 Previous Studies

An N-Ring SiGe HBT is formed by the incorporation of a "dummy collector" or "N-Ring," n+ implant around the perimeter of the trench isolation of an NPN SiGe HBT [106, 96]. A cross-section comparison of a standard SiGe HBT and an N-Ring SiGe HBT is presented in Figure 49. The additional reversed-biased junction formed by the N-Ring-substrate serves to shunt generated carriers, from ion strikes through the substrate, away from the sensitive subcollector-substrate junction. This technique

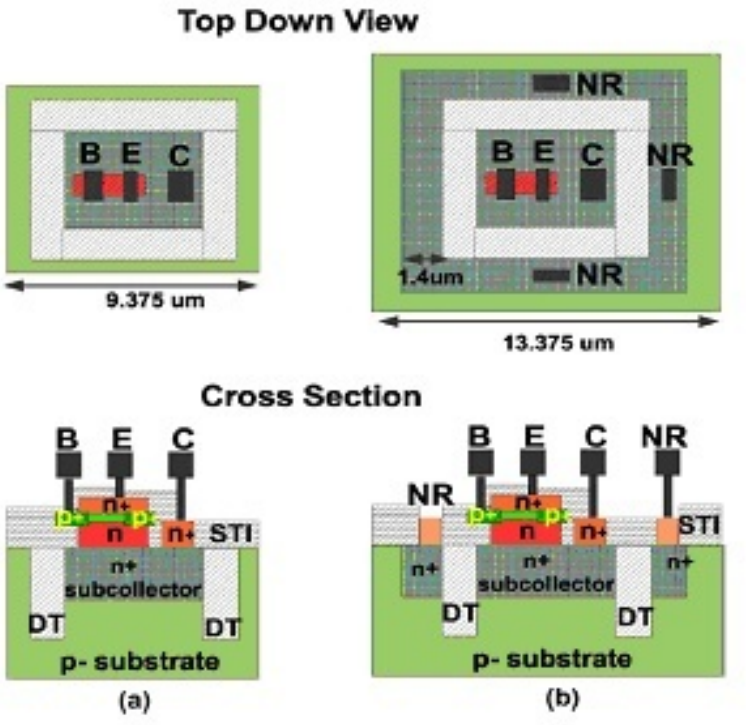


Figure 49: Top down and cross-sectional views of the (a) standard SiGe HBT and the (b) N-Ring variant from [70].

is theorized to be most effective for ion-strikes occurring outside the trench isolation of the HBT, reducing the total sensitive area to transient effects while having a minimal impact on the transient profiles of ion-strikes within the active area (especially emitter-center) of the HBT. To date, primarily only single transistor studies have been performed on this RHBD technique, using ion beam induced charge collection (IBICC) measurements by means of a heavy-ion microbeam [22]. These experiments show promising results for reducing peak collector charge collection as well as shrinking the sensitive area of the device as illustrated in Figure 50. The trend in nearly eliminating collector-induced charges for ion-strikes external to the trench isolation of the HBT is seen across several industry platforms. A second fact from this figure to be discerned is that the collector-induced charge for ion-strikes through the center of the active area of the device is reduced for this technology with shallower trench isolation when N-Rings are employed. This result appears to directly supplement the work in analyzing the impact of DTI depth in SEE response from the previous chapter.

Despite these promising IBICC results, in order to truly evaluate the efficacy of mitigating single event effects through the incorporation of an N-Ring SiGe HBT, it

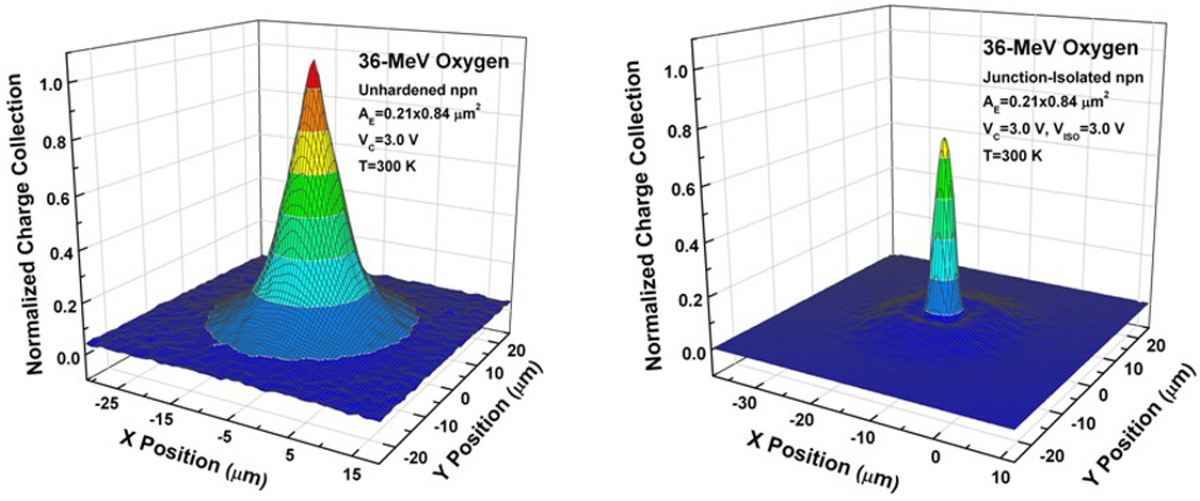


Figure 50: Normalized (to peak charge of standard device) charge collection measurements of the (a) standard SiGe HBT and the (b) N-Ring SiGe HBT performed using SNL's 36 MeV ^{16}O microbeam from [22].

is necessary to test circuits which contain these structures. N-Ring SiGe HBTs were integrated into both an analog (a SiGe bandgap reference) and a digital (a 16-bit standard master/slave serial shift register) circuit and tested in-beam. These circuits were designed and developed using IBM's 1st generation (f_T of 46 GHz and f_{max} of 65 GHz) SiGe BiCMOS platform. The analog circuit results have been reported previously [70], whereas the digital circuit results are shown here for the first time. Given the significant reduction in measured sensitive area and total peak collector charge collection of the N-Ring HBTs reported for the IBICC results, it would be expected that the digital systems built from these structures would show improved error performance in a heavy-ion broadbeam environment.

4.2 Experimental Results

The digital circuits tested include two 16-bit master/slave serial shift registers, one composed of standard SiGe HBTs and the second built with N-Ring SiGe HBTs. The registers were completely identical in their architecture, clock distribution, operation frequency, and power dissipation. These circuits were irradiated at Texas A&M's Cyclotron Institute's heavy-ion broadbeam facility and tested in-beam with an Agilent MP1764 bit error rate testbed (BERT) utilizing a 127-bit pseudo-random input data sequence. The registers were operated with a 5.2 V rail (the N-Rings were held at this potential) and at a frequency of 1.6 Gbps. Bit upsets and the total fluence were recorded during exposure, permitting the construction of a full error cross-section curve. The TAMU facility provided a wide range of very high-energy ions with various LETs that have no recorded spatial correlation with strike events. Heavy ion exposures included 15 MeV/u ^{197}Au, ^{129}Xe, ^{84}Kr, ^{40}Ar, ^{20}Ne and 25 MeV/u ^{22}Ne giving linear energy transfers (LETs) of 86.5, 52.2, 28.4, 8.5, 2.7, and 1.8 MeV-cm^2/mg respectively. All DUTs were exposed at normal incidence at room temperature.

The measured error cross-section curves generated for both standard and N-Ring

shift registers are plotted in Figure 51. The error bars associated with the measurements overlap with the data points when plotted on a log-linear scale. While the threshold linear energy transfer (LET) for both registers is identical, the saturated error cross-section is larger for the N-Ring SiGe shift register. This result is counter-intuitive in light of the results from the single-device IBICC studies performed on N-Ring SiGe HBTs. With the significant measured reduction in sensitive area and total peak collected charge of the N-Ring HBTs reported for the IBICC results, it would be expected that the N-Ring shift register would show improved error performance. To verify this result, another set of the two circuits were packaged and brought to LBNL for additional broadbeam testing. A 10 MeV/u ion beam cocktail was used to test the SEU cross-section of both sets of shift registers operating at 1 Gbps. In addition to normal incidence data, the part was rotated to achieve a 30ngls on incidence. The voltage on the N-Ring terminal was also varied, with the values of -2.2 V, -4.2 V and floating (no applied bias) employed. The measured error cross-section for this data

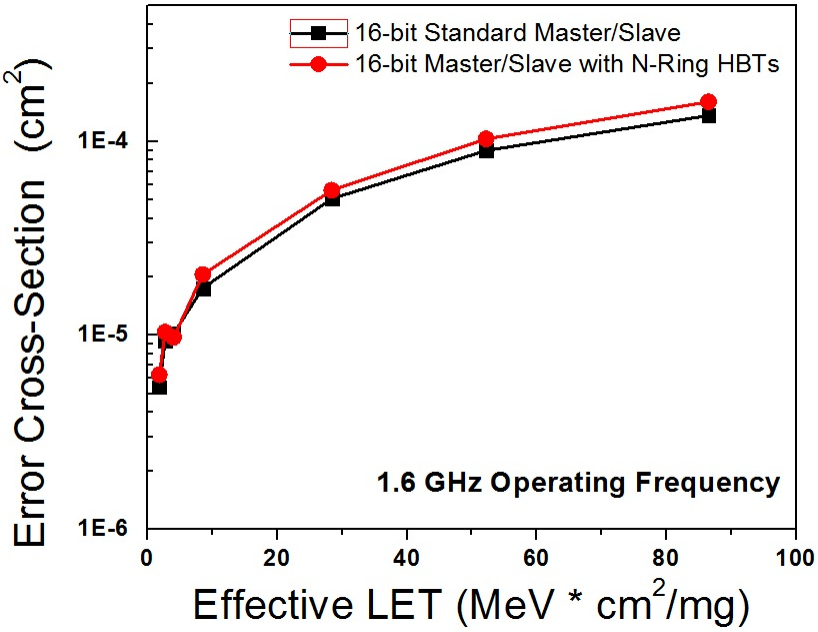


Figure 51: Error cross-section curve for a standard and N-Ring variant 16-bit SiGe shift register operating at 1.6 Gbps.

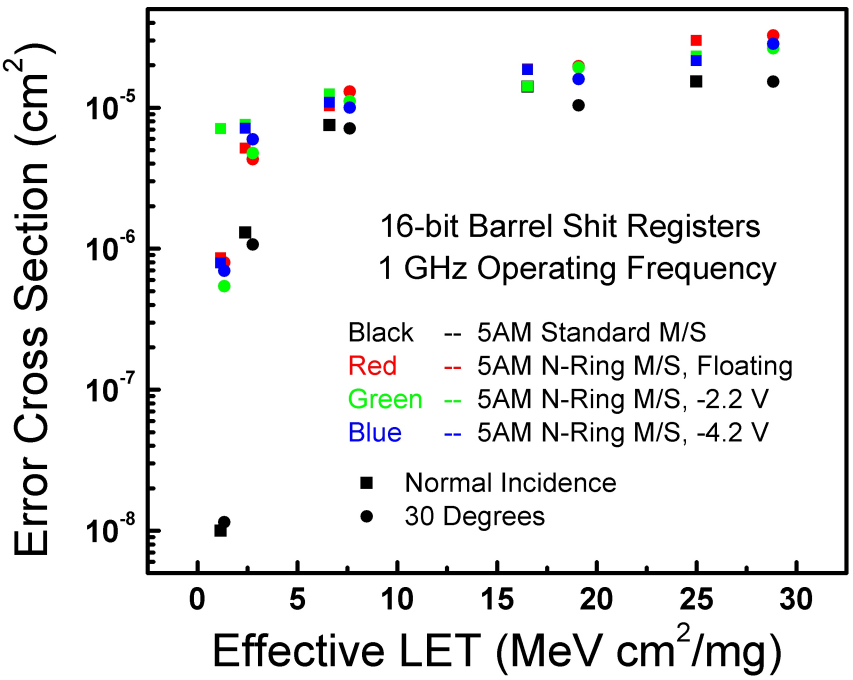


Figure 52: Error cross-section curve for a standard and N-Ring variant 16-bit SiGe shift register operating at 1 Gbps for two meaured angles and multiple applied N-Ring biases.

plotted as a function of effective LET is show in Figure 52. This data confirms the initial tests, with the N-Ring shift register showing an elevated cross-section for all applied biases of the N-Ring terminal, and all measured angles.

This discrepancy has been also been observed between IBICC measurements and circuit results for analog voltage regulators [70]. The voltage references built with SiGe N-Ring SiGe HBTs showed additional sensitive regions to transient phenomena that were no present in the voltage references constructed with standard SiGe HBTs. However, the N-Ring voltage reference showed a reduction in the number of transient events with large amplitudes. To interpret the complex set of results captured from the digital circuit exposures and explain the discrepancy between the single-device IBICC measurements, time resolved ion-beam induced transient current (TRIBIC) experiments were performed on single SiGe HBTs with and without N-Rings.

The TRIBIC method directly captures the induced current transient waveforms on

all device terminals due to an ion strike event, providing information on the transient's amplitude, polarity, and duration. An easy visualization of the results of a TRIBIC measurement can be created by mapping the peak transient amplitude of a specified terminal as a function of the recorded position of the transient event. The primary sensitive terminal for the circuits we have tested is the collector; therefore, this terminal was selected for imaging the transient response. The transient map for the standard device is shown in Figure 53, whereas the transient map for the N-Ring device is shown in Figure 54. A comparison of the two maps clearly shows that the N-Ring HBT has a much larger sensitive area for transients on the collector terminal. These results are a striking contradiction to earlier IBICC measurements that have shown reductions in the sensitive area of an N-Ring HBT [96, 22].

Despite the difference in total sensitive area, both devices show the same characteristics for transients induced by ion strikes internal to the deep trench; namely, the peak transient collector current is negative in polarity, indicating current flowing into the collector terminal. The most sensitive region for maximum transient signatures within the deep trench is through the emitter of the device, where a normally incident ion will pass through all the sensitive junctions. Figure 55 presents a comparison between the collector transient signals for each device type due to emitter-center strikes. These transients are similar, with slight reductions in peak amplitude for the N-Ring device. The magnitude of this reduction will vary depending on the depth of the deep trench isolation layer, with shallower trenches resulting in greater attenuation.

The difference in sensitive area between the two device types arises from the presence of collector transients external to the trench isolation for the N-Ring HBT. These signals have maximum peak transient amplitudes that are positive in polarity, opposite to that of strikes occurring internal to the trench isolation. The area of maximum sensitivity for these positive polarity transients occurs for ion strikes directly through the N-Ring-substrate depletion region. It can be thus be inferred that there is

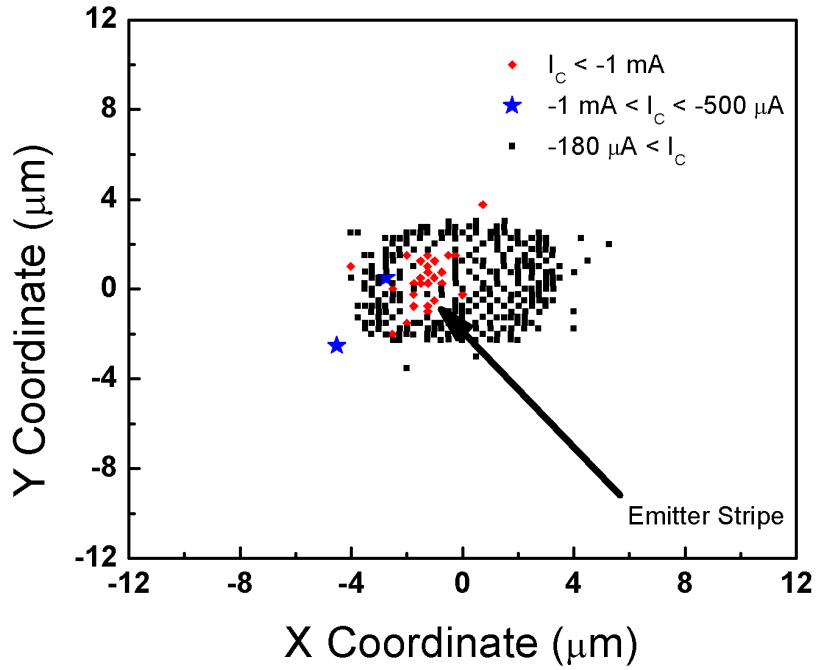


Figure 53: Peak transient collector current amplitude plotted against the X-Y coordinates of the ion strike position for a standard SiGe HBT.

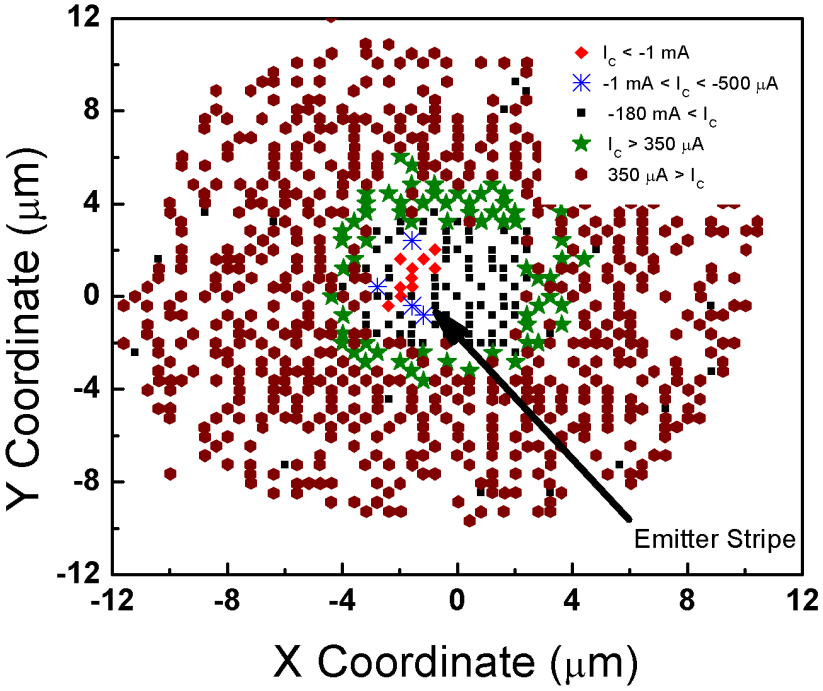


Figure 54: Peak transient collector current amplitude plotted against the X-Y coordinates of the ion strike position for an N-Ring SiGe HBT.

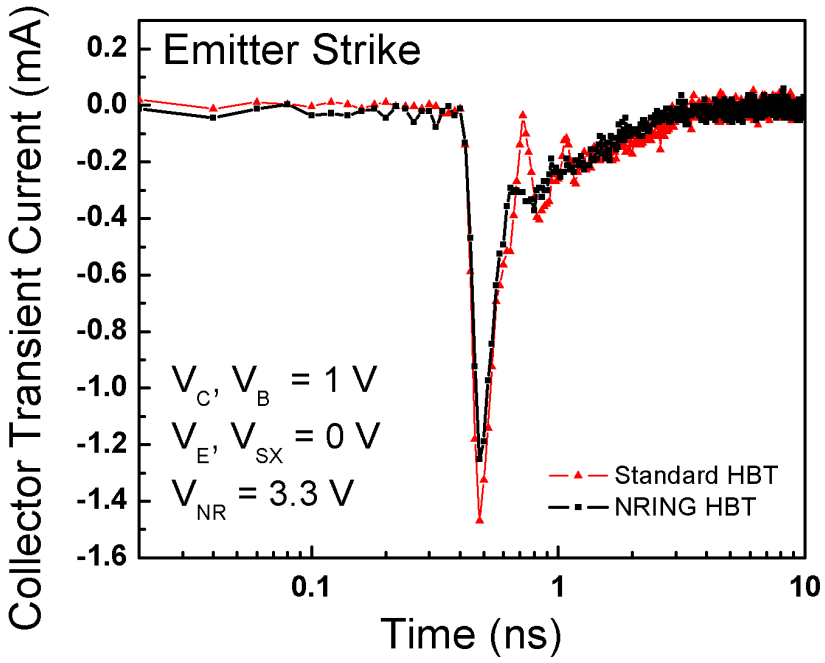


Figure 55: Measured transient waveforms on the collector terminal induced by an emitter ion strike for both a standard and N-Ring SiGe HBT.

a coupling phenomena occurring between the device collector and the N-Ring terminal. In Figure 56, typical transient waveforms arising from a normally incident oxygen ion strike to the N-Ring region for the collector, base, N-Ring, and substrate terminals are plotted. As reflected in the transient map, the collector transient has a peak amplitude that is positive; in addition, the collector signal has a bipolar signature. This bipolar nature of the collector transient waveform accounts for the discrepancy between the TRIBICC and IBICC results. The IBICC set-up requires charge-sensitive preamplifiers which integrate the transient waveforms to give a measure of the total charge induced on a device terminal and are limited to only unipolar signals. Bipolar signals will potentially lead to cancellation of integrated charges, giving erroneous values of total induced charge in an IBICC experiment. To explain the experimental results 3-D TCAD models were compiled using CFDRC's finite element modeling software, NanoTCAD.

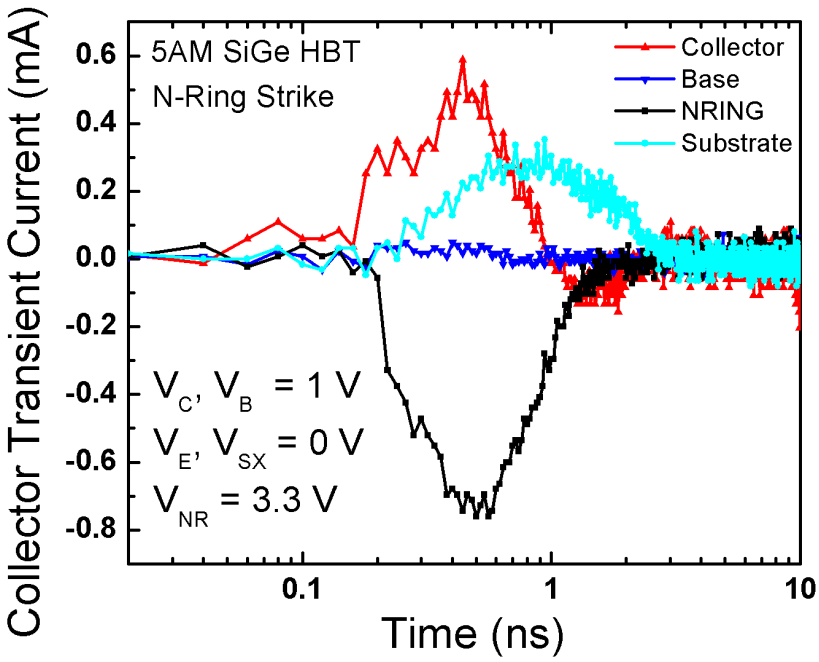


Figure 56: Measured transient waveforms induced on the collector, base, N-Ring, and substrate due to an N-Ring ion strike of an N-Ring SiGe HBT. The collector transient displays a bipolar signature.

4.3 3D TCAD Modeling

The ion strike simulations were performed using an ion LET of 7 MeV-cm^2/mg and a penetration depth of 25.4 μ m in the bulk silicon (calculated in SRIM using the front side metal stack thickness), roughly modeling the ^{16}O ion used at SNL. The strike location was chosen to be through the N-Ring, external to the DTI of the device. The biases on the emitter, substrate, and base were fixed at ground (given that external trench responses will only be dictated by the collector, substrate and N-Ring), while the N-Ring was held at 3.3 V. Multiple simulations were run with varying collector voltages (0 V, 1.0 V, and 3.3 V) in order to determine the bias dependence of the transient response. In Figure 57 and Figure 58 the transients induced on all terminals for a device with a collector held at 0 V and 3.0 V, respectively, are plotted as a function of time. For NanoTCAD, the polarity of terminal currents is determined by the current directionality at the model interfaces, with positive current indicating

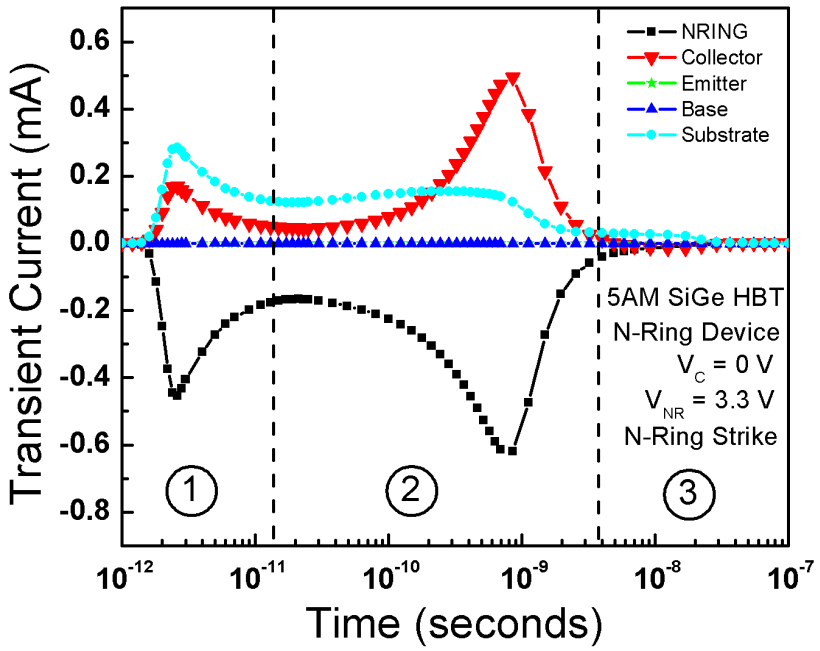


Figure 57: Simulated transient waveforms for an ion strike through the N-Ring of an N-Ring SiGe HBT biased with 3.3 V on the N-Ring and collector and with all other terminals ground.

current flowing out of the three dimensional model boundary and negative flowing into the model boundary. Directly following the ion strike, current flows out of the collector terminal of the device (analogous to electrons flowing into the collector terminal). Near the conclusion of the transient signal, however, the polarity is swapped as current flows into collector (electrons flowing out of the terminal). In order to analyze the transient response, it is necessary to break the signal into different regions. The presence of these regions in the transient signature is dependent on terminal biases, as can be observed by comparing Figure 57 and Figure 58.

4.3.1 Region 1

The first region of the transient waveform occurs nearly instantaneously following the ion strike and is essentially identical between both collector bias conditions. As the ion passes through the semiconductor material, it ionizes a dense concentration of electron-hole pairs. The charge carriers ionized within the depletion region of the

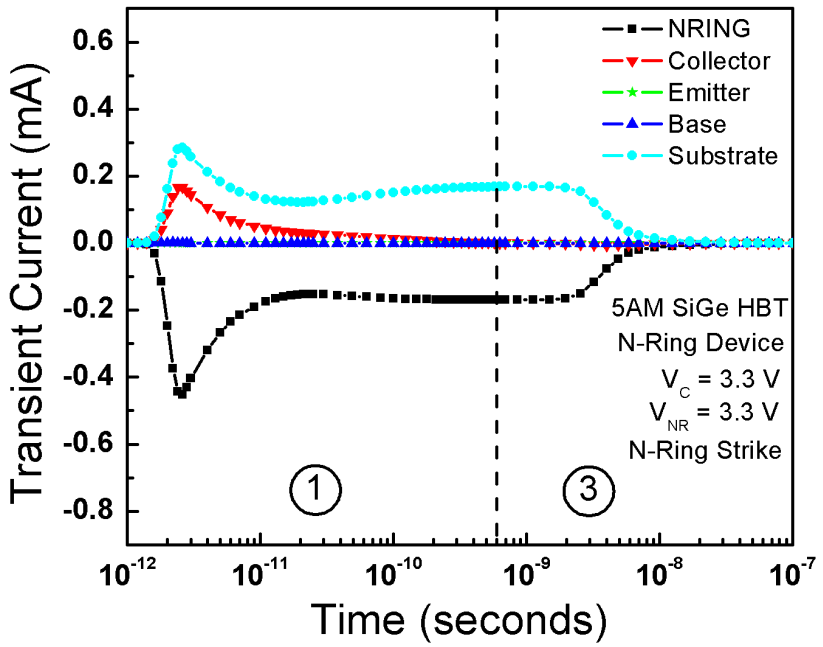


Figure 58: Simulated transient waveforms for an ion strike through the N-Ring of an N-Ring SiGe HBT biased with 3.3 V on the N-Ring and with all other terminals ground.

N-Ring-substrate junction are separated by the electric field. Electrons are pulled out of the N-Ring contact while holes are dumped into the lightly doped substrate. These excess holes begin to diffuse to the subcollector-substrate junction and accumulate, as they are pushed back by the electric field of this junction. This junction acts as a capacitor, balancing the gathering positive charges by pulling electrons into the 3-D model from the collector contact to the collector side of the subcollector-substrate junction. In Figure 59, the time evolution of the build-up of excess free carriers is plotted along a vertical slice through the device. The number of excess carriers is calculated by the difference in carrier concentration at steady state prior to the strike, and at a given time step. Given how quickly the carrier interaction occurs within this region (10 ps), the measurement set-up will be unable to capture this transient response since the sampling rate of the oscilloscope is limited to 20 ps/sample

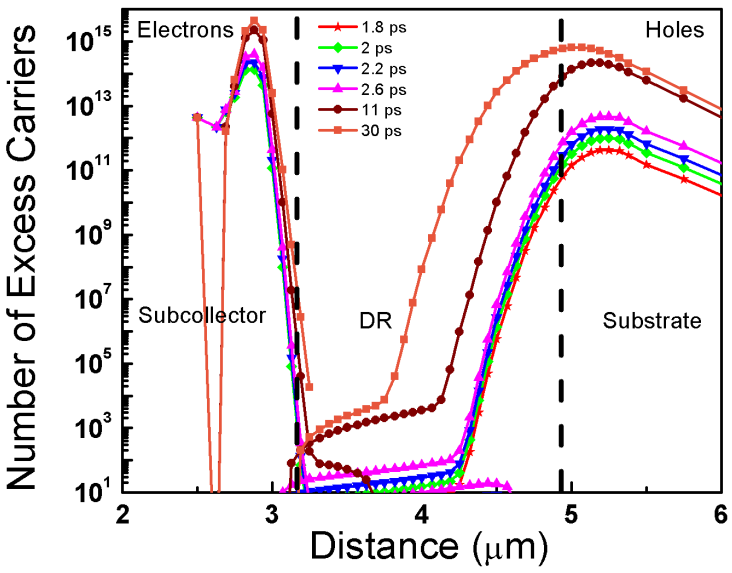


Figure 59: Excess electron and hole concentrations following an ion strike on either side of the depletion region (DR) of the subcollector-substrate junction.

4.3.2 Region 2

The transient shifts from region 1 to region 2 as the substrate potential sufficiently modulated to turn on the parasitic NPN transistor formed by the N-Ring-substrate-collector. This process has been termed "funneling" in the literature and describes the collapse of a junction as a result of a sudden flood of free charge carriers and the subsequent push-out of electric field lines (potential gradient) to maintain the fixed voltage drop applied to contacts [39, 20]. In this case, the N-Ring-substrate junction collapses as a result of an ion strike, raising the potential of the bulk substrate. In Figure 60 a cross-section of the modeled device displays the potential contours through the substrate, at a time corresponding to the peak collector current induced within region two (0.86 ns) of Figure 58. At this point, the substrate potential has been raised such that the subcollector-substrate junction becomes forward biased, acting as the emitter-base junction of the parasitic bipolar transistor. A forward current of electrons flows from the collector to the N-Ring terminal until the N-Ring-substrate junction re-establishes itself, lowering the substrate potential and turning off the parasitic

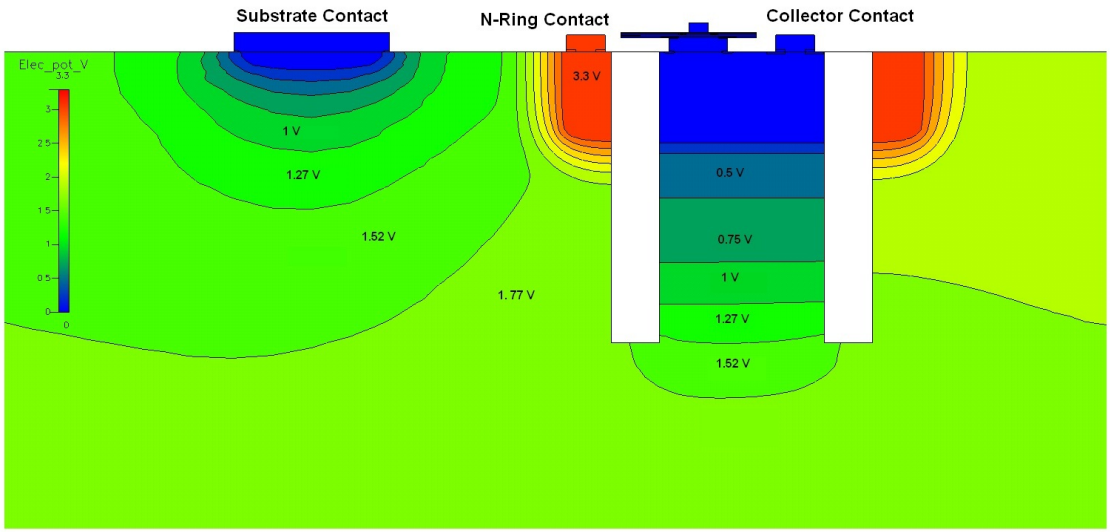


Figure 60: Cross-sectional view of an N-Ring HBT showing the potential contours through the substrate occurring 0.86 ns after an N-Ring centered strike.

device. This region of the transient signal is highly dependent on the terminal biases, as reflected in Figure 57 and Figure 58. If a sufficient reverse-voltage bias is applied to the collector-substrate junction, the potential modulation of the substrate will not be sufficient to forward-bias this junction to turn the parasitic NPN transistor on.

4.3.3 Region 3

In the final region of the transient, the polarity of the collector signal flips. Electrons which have been ionized deep in the lightly doped substrate have now diffused from the strike path and reached the subcollector-substrate junction. As has been discussed previously, with the low-doped substrate, free carriers are able to diffuse a very large distance before experiencing recombination events. As electrons diffuse to the depletion region boundary they are swept across by the electric field and pulled out of the collector terminal. This section of the transient waveform is consistent with the Ramo-Schockley theorem discussed in Chapter 2.

4.4 Conclusions

The impact of N-Rings on SiGe HBTs has been fully explored, uncovering the complex transient responses and bias dependencies. By collapsing the data taken from both digital circuit experiments and single-device TRIBIC measurements, some significant conclusions can be drawn. The conclusions will have impact on the design of radiation tolerant SiGe circuits. It has been shown that single and multiple bit upsets are increased when incorporating N-Ring SiGe HBTs into the latch architecture. Typically, for ion-strikes to an HBT, the HBT collector sinks transient current, resulting in the pulling of nodes from a high potential to a lower one (often denoted as altering a digital state "1" to a digital state "0"). For the case of the N-Ring SiGe HBT, if an ion strikes through the N-Ring terminal, the HBT collector will source current, raising the nodal potential. An additional mode of latch upset is now introduced with the possibility of a digital "0" becoming a digital "1" after a strike. As reflected in the error cross-section measurements of Figure 49, this new sensitivity will result in nearly double the errors for an N-Ring HBT register. Consequently, the impact of incorporating N-Ring HBTs into circuit designs is strongly dependent on circuit topology (e.g., analog vs. digital), the important failure modes, and overall system sensitivity.

CHAPTER V

INVERSE-MODE CASCODE SIGE HBTS

5.1 Device Description

The inverse-mode operation of a device is the operation of a bipolar transistor with the emitter and collector terminals electrically swapped. This mode suffers from some inherent limitations, which include reductions in both device gain (given the lower doped, single crystal physical collector as compared to the polycrystalline emitter) and maximum operational speed (larger emitter capacitances and base width) when compared to standard forward mode operation. However, with technology scaling the inverse mode performance has increased, given that doping levels increase with vertical scaling and capacitances shrink with lateral scaling [3]. Recently, the incorporation of inverse-mode devices in radiation intensive applications has been investigated [4]. This move is motivated by the potential built-in SEU mitigation of inverse mode operation. When the physical emitter is operated as the electrical collector, the substrate becomes decoupled from the output node (collector terminal in CML logic). The most sensitive junction becomes the electrical emitter (physical subcollector-substrate junction), which collects the majority of the charge generated in the semiconductor bulk. A significant system speed penalty is paid, however, for incorporating inverse mode devices in a design.

The inverse-mode cascode SiGe HBT is composed of two transistors combined onto a single shared subcollector as depicted in the cross section of Figure 61 (a), while the schematic of the structure is shown in (b) [100]. This structure is similar to a typical cascoded transistor pair where transistor Q1 is operated as a common-emitter amplifier and Q2 operates in the unity-current gain, common-base mode.

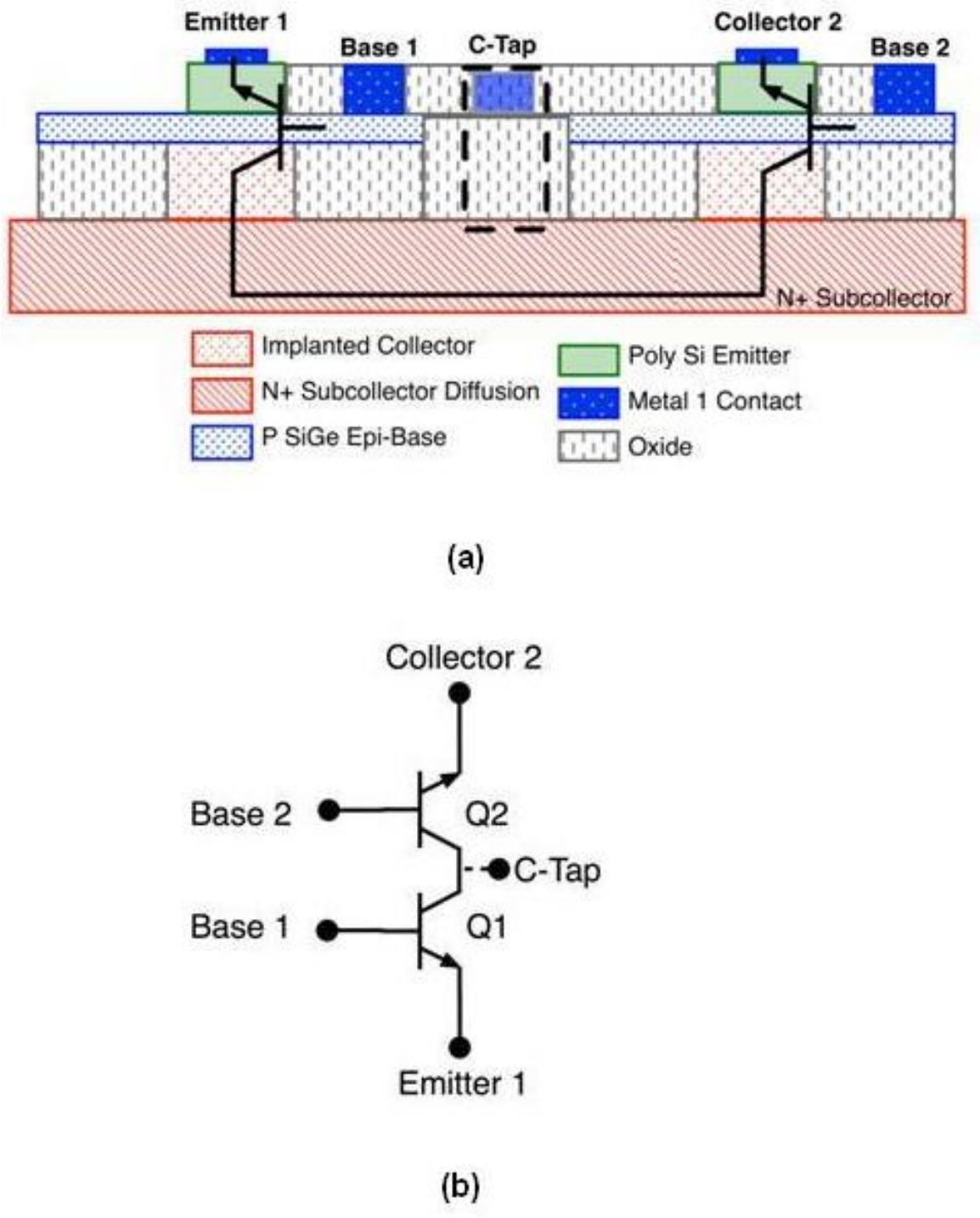


Figure 61: A cross section of the inverse-mode cascode device revealing its shared subcollector design is given in (a) while the joint device schematic is given in (b).

With sufficient voltage headroom (two V_{BE} drops at minimum) the structure can be operated as a standard, single device. The input signal is applied to the lower base

terminal (Base 1), resulting in amplified current flow through the collector terminal (Collector 2). To accommodate the "shared-subcollector" design of our cascode topology, transistor Q2 must be operated in the inverse mode. Similar to inverse-mode operation of a stand-alone device, it is expected that the electrical swapping of the emitter and collector will provide the decoupling of the output terminal and the sensitive subcollector-substrate junction, promoting built-in SEU mitigation. An additional variant of the structure incorporating a contact to the buried subcollector (referred to as the C-Tap terminal) was investigated.

Although the proposed structure integrates two stand-alone SiGe HBTs, no area penalty exists when comparing the enclosed deep trench area of an inverse-mode cascode SiGe HBT with that of a single stand-alone SiGe HBT in a C-B-E-B-C layout. A slight error penalty exists for inverse-cascode structures where transistor Q2 has been optimized for inverse mode operation (a slight increase in deep trench enclosed area). The optimized inverse-mode cascode device [3] exhibits significantly improved values of f_T as compared to a standard inverse mode device, as seen in Figure 62.

Despite an optimized inverse-mode device only having a peak f_T of approximately 10 GHz (over an order of magnitude smaller than forward mode operation!), the optimized inverse-mode cascode device has a peak f_T of nearly 100 GHz. This performance was measured on standard SiGe HBTs sized with an emitter area of 0.12 x 2.5 μm^2 and inverse-mode cascode SiGe HBTs with Q1 sized with an emitter area of 0.12 x 2.5 μm^2 and Q2 sized with a physical emitter area of 0.12 x 5.0 μm^2. With this boost in device speeds, system performance would not have to be sacrificed to obtain mitigation to SEU; however, the SEU susceptibility of these devices still needs to be investigated.

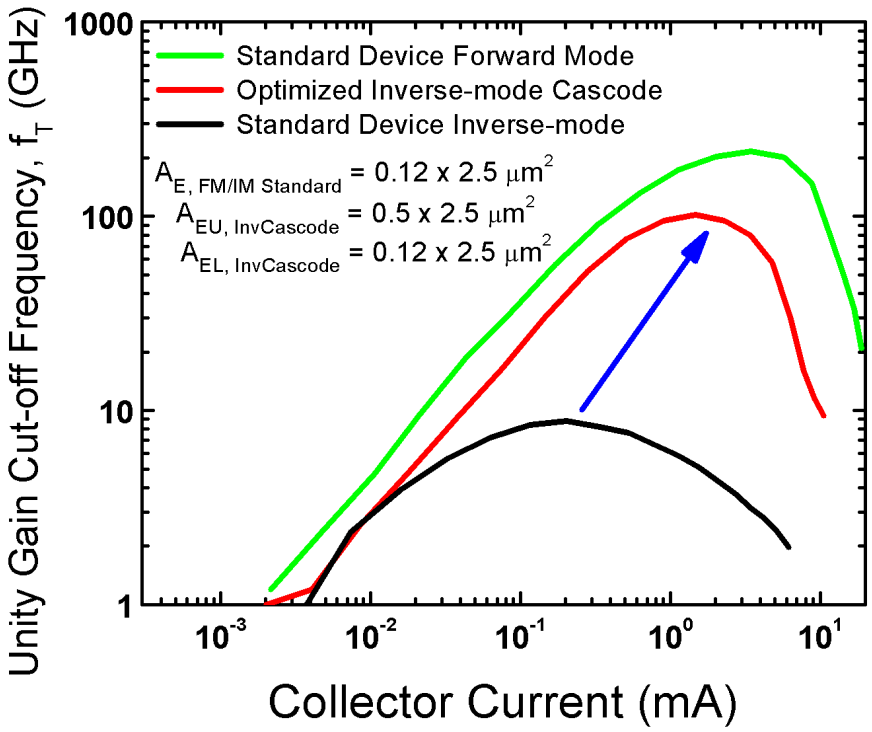


Figure 62: Comparison of unity gain cut-off frequency for a standard device, an inverse mode device, and the inverse-mode cascode device.

5.2 Device-Level Radiation Sensitivity

Given that this structure is completely innovative and has not been analyzed in any context, both TID testing and heavy ion microprobing were performed on devices fabricated with this topology in IBM's 3rd generation, 8HP technology. The total-dose testing was performed at Vanderbilt University using a 10 keV X-Ray ARACOR test bench. Pre and post-irradiation dc measurements were performed so that any degradation in the collector or base currents could be captured. Only a single dose point of 1 Mrad(SiO_2), well above the total sustained dose for typical orbital missions, was captured as a comparison point for pre-radiation measurements. Also, given that only an X-ray source was utilized, no information on displacement damage could be discerned from the data. However, from past experiments it has been shown that displacement damage does not have a significant effect on the standard operation of these 3rd generation SiGe HBTs.

The second set of experiments performed was aimed at quantifying the SEU vulnerability of these new structures. Charge collection statistics of two device variants and different biases were obtained using SNL's Nuclear Microprobe Facility. Both the standard inverse-mode cascode SiGe HBTs as well as the inverse-mode cascode SiGe HBT with reach-through subcollector contact (C-Tap) were irradiated. A 36 MeV ^{16}O ion beam was used. IBICC measurements were performed on all device terminals of the devices irradiated. The standard inverse-mode cascodes were irradiated under two separate bias schemes: 1) with all terminals grounded except for the substrate held at -4 V (a bias condition allowing direct comparison to previous microprobe data on standard single SiGe HBTs), and 2) 2 V on both the collector and upper base and -4 V on the substrate, with all other terminals grounded. The inverse-mode cascode with C-Tap was irradiated with only a single bias condition, specifically 2 V on the collector, upper base, and C-Tap, -4 V on the substrate, and all other terminals held at ground.

5.2.1 TID Testing

The forward-mode Gummel characteristics of the inverse-mode cascode SiGe HBT measured pre and post 10 keV X-ray radiation is shown in Figure 63.

The response of this new device shows the same damage characteristics as standard devices in SiGe technologies. The increase in base leakage is evident for both the upper and lower bases of the inverse-mode cascode. Also, no change in the collector current is measured after exposure to X-rays. The larger excess base current density for the upper base (base of Q2) is attributed to the inverse-mode operation of the SiGe HBT. For inverse-mode operation the sensitive oxide interface to radiation damage is the STI oxide. This oxide characteristically has a much larger overlap over the electrical emitter-base junction (physically the collector-base junction), which leads to a greater sensitivity to defect-induced G/R leakage currents [97]. Given that the input signal is

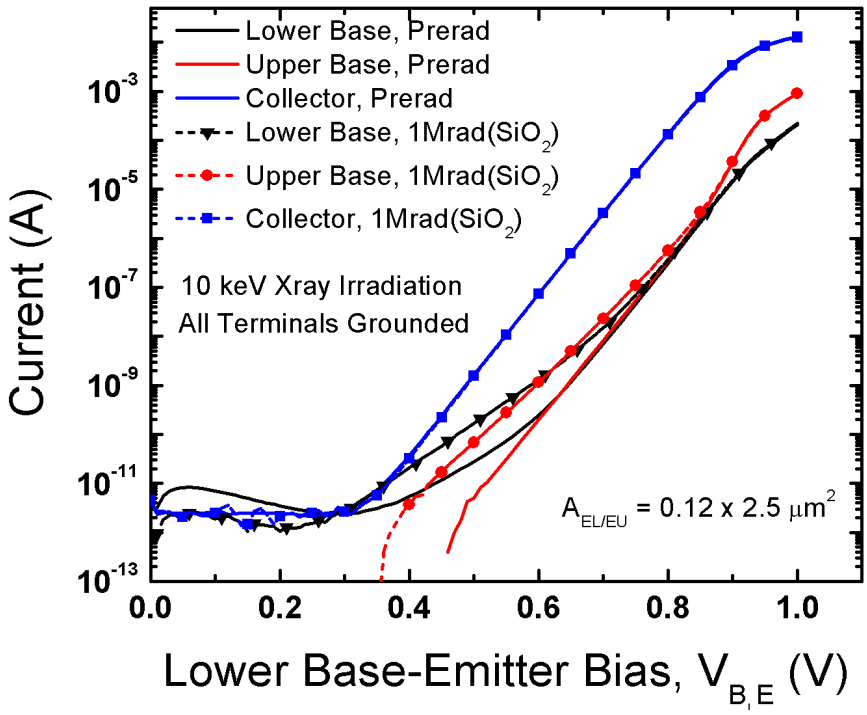


Figure 63: TID response of the standard inverse-mode cascode to 10 keV X-rays. Noticeable excess base current is seen at low injection levels, but quickly falls away as biases approach standard "on" biases for circuit applications.

applied to the lower base terminal, the gain of the device is measured from the ratio of the lower base current to the collector current. The increase in base leakage of the upper base node is therefore irrelevant for gain calculations. Additionally, nominal "on" base-emitter biases will be on the order of ≈ 0.85 V, a bias region where no excess base current is evident in the inverse-mode cascode.

5.2.2 Heavy-Ion Microprobing

The IBICC measurements obtained from heavy ion microprobing revealed very interesting and exciting results. Given that the output of digital CML is the collector terminal, this will be the only terminal where data is reported. The first device presented is the standard inverse-mode cascode SiGe HBT exposed under the two different bias configurations described previously. This data is overlay-ed with charge collection data on the collector of a device using a standard architecture and with a bias scheme

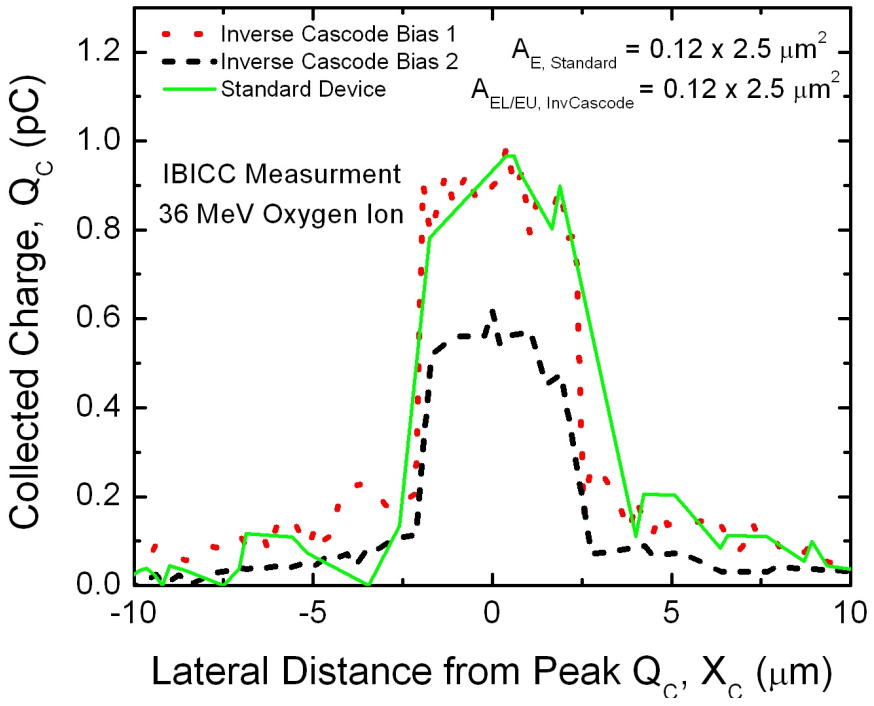


Figure 64: Measured 2-D cut of the electrical collector-collected charge data for the inverse-mode cascode subject to two bias schemes, overlayed with standard device charge collection data.

of all terminals grounded. A 2-D cut of the integrated charge collection data of the electrical collector terminal (for both biases of the inverse-mode cascode and the standard device), collapsed on the X-Y plane with one coordinate held constant is found in Figure 64.

There are two important pieces of information to be extracted from this figure. The first is that when the inverse-mode cascode device is irradiated under bias scheme 2, the response overlays with the response to a standard device of equal dimensions. At first this might come at a surprise, given that the output terminal (electrical collector) is isolated from the subcollector-substrate junction, however if we consider the biases applied, we can make sense of the response. For bias scheme 2, electrons that accumulate in the subcollector of the device after being funneled by the subcollector-substrate junction must either recombine in the subcollector, or diffuse into either the upper or lower bases. After diffusing they will then be collected

by either the collector/emitter by drifting across the base-emitter/collector junction. The impedances seen by electrons for traversing these two paths are not equivalent. The energy barrier for majority carrier (electron) diffusion of the upper base-emitter (physical collector) is lower than that of the lower base-emitter junction. This results from the subcollector being forced to 2 V to keep Q2 from turning on (Q1 is biased into an off state, which blocks current flow). This forced potential will reverse bias the lower base-emitter junction since the lower base is being held at 0 V. The bias actively applied to the upper base is 2 V, so the only potential across this depletion region is the built-in potential of the junction.

The second important fact to glean from this data is that a drastically different response is seen for the bias scheme where all the device terminals are grounded. For this bias, the inverse-mode cascode SiGe HBT shows approximately one-half the total collector-collected charge on the electrical collector terminal when compared to a standard HBT. Once again, understanding the potentials applied and the affect on the energy barriers for free carriers is key to understanding this result. For bias scheme 2, all terminals have 0 V applied to them, so equivalent impedances are seen between the upper subcollector-base junction and the lower subcollector-base junction. It is expected that charge will split evenly between these two paths and be collected equally on the collector and emitter terminals.

The second set of results to be presented and analyzed are the charge collection statistics of the inverse-mode cascode SiGe HBT where the C-Tap is present and biased. These results are shown in Figure 65. For this structure, almost complete elimination of charge collection on the electrical collector terminal is displayed. Almost all of the electrons collected by the subcollector-substrate junction are present on the C-Tap terminal, evidenced by the overlying charge collection profiles for the C-Tap and substrate terminals. Unlike the standard inverse-mode SiGe cascode, free electrons which are collected from the substrate-subcollector junction are quickly able to be

removed by the C-Tap contact. For the standard devices, charges accumulate in the subcollector and then diffuse across junctions to be collected be either the emitter or collector terminals.

5.2.3 3D TCAD Modeling

To validate the experimental results obtained from microbeam testing, the inverse-mode cascode SiGe HBT was built using the calibrated 8HP device deck created from the previous DTI study. CFDRC's NanoTCAD software was employed to simulate ion strike events on these custom devices. All strike simulations utilized an ion LET of 5.4 MeV-cm^{2}mg to reflect the LET of the oxygen ions used at Sandia National Laboratory. Strike simulations were executed for the same device types (standard inverse-mode cascode and inverse-mode cascode with C-Tap) and the same biases. Unlike the standard HBT where the most sensitive strike location is the center of the emitter, the most sensitive strike location for the inverse-mode cascode HBT is

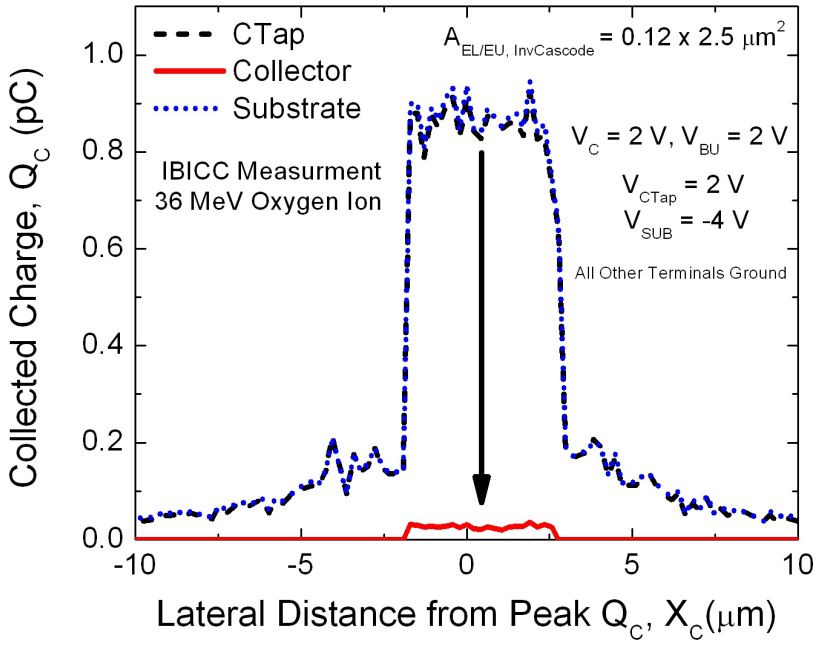


Figure 65: Measured 2-D cut of the electrical collector-collected charge data for the inverse-mode cascode with C-Tap showing nearly complete mitigation of charge collection on the electrical collector terminal.

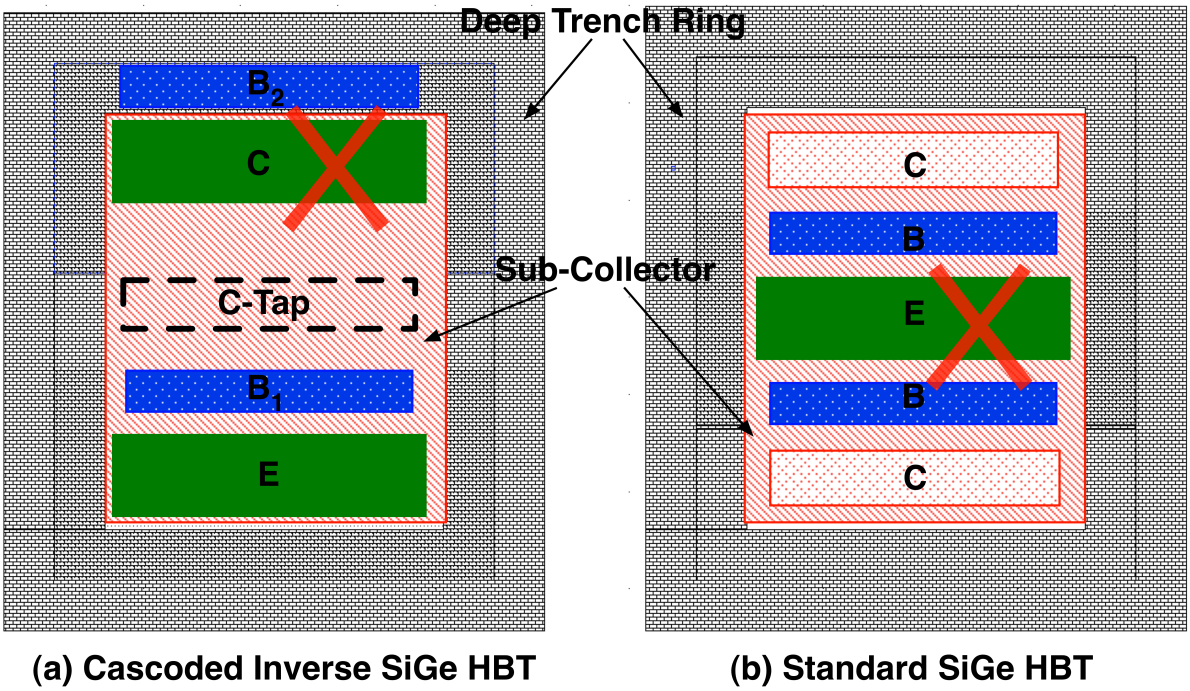


Figure 66: Top down comparison of (a) inverse-mode cascode device showing the two variants and (b) a standard device. The most sensitive ion strike locations are shown for each structure with a red "X".

determined to be the center of the electrical collector (the upper physical emitter), given that an ion will pass through the depletion regions directly tied to the output terminal of the device. These two most-sensitive strike locations for the two different device types are illustrated in the top-down view given in Figure 66.

The bias scheme that was simulated under an ion strike condition was bias scheme 1, where the upper base and collector are held at 2 V and the other terminals are held at 0 V (except the substrate which is held at -4 V). The transient current waveforms which are generated on all device terminals is shown in Figure 67, and the resulting integrated charge profile is displayed in Figure 68.

The charge collection profile of the electrical collector terminal from the simulation is in agreement with the experimental data shown previously in Figure 64. Nearly all electron charge is collected on the collector terminal, with minimal charge induced on the emitter terminal. Referencing the current waveforms in Figure 67, it is obvious that

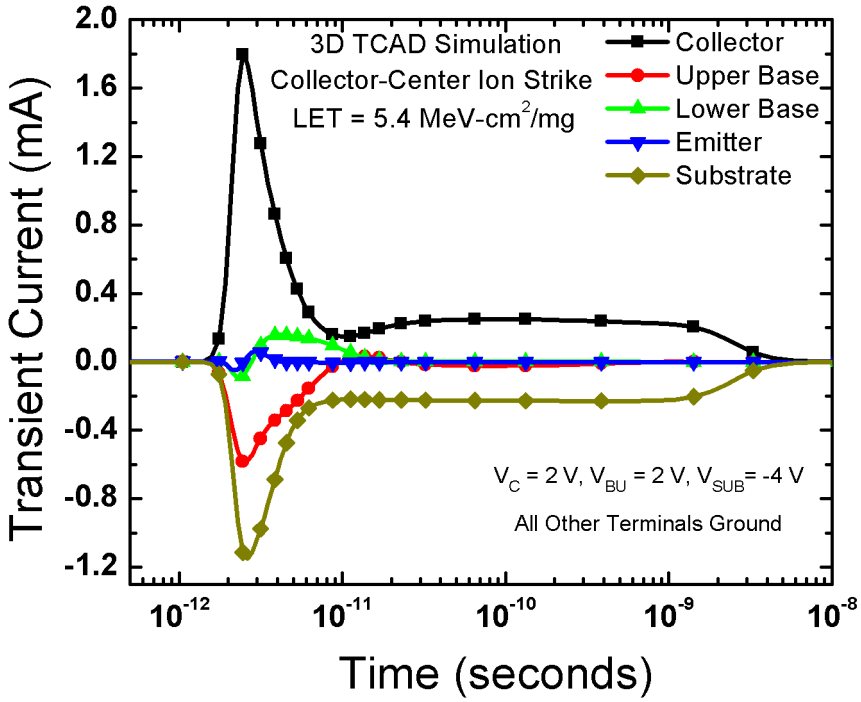


Figure 67: Simulated current transients for every device terminal of an inverse-mode cascode SiGe HBT as a result of an ion strike to the center of the collecter while subjected to bias scheme 2.

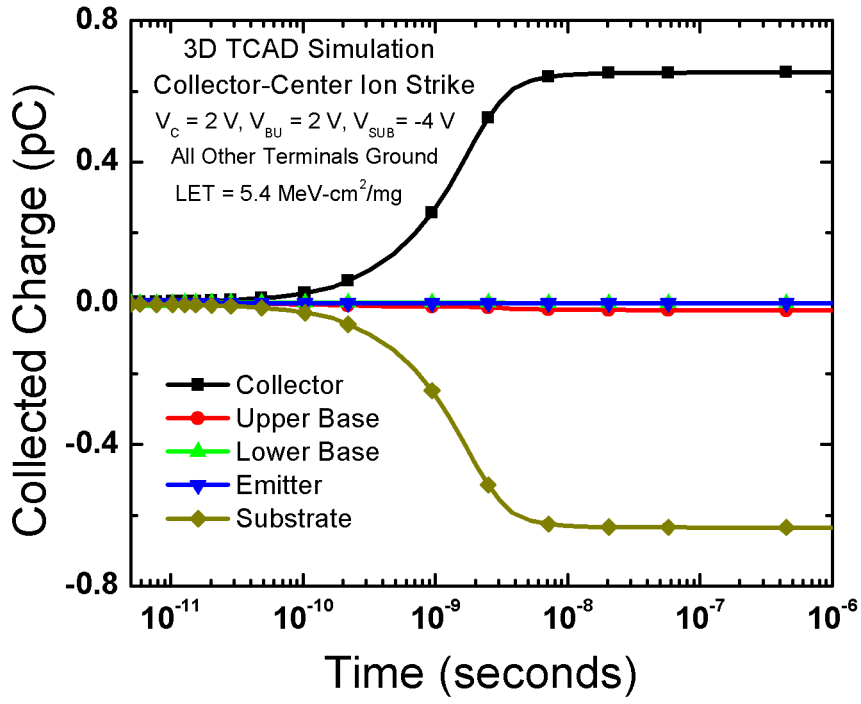


Figure 68: Integrated collected charge for every device terminal of an inverse-mode cascode SiGe HBT as a result of an ion strike to the center of the collecter while subjected to bias scheme 2.

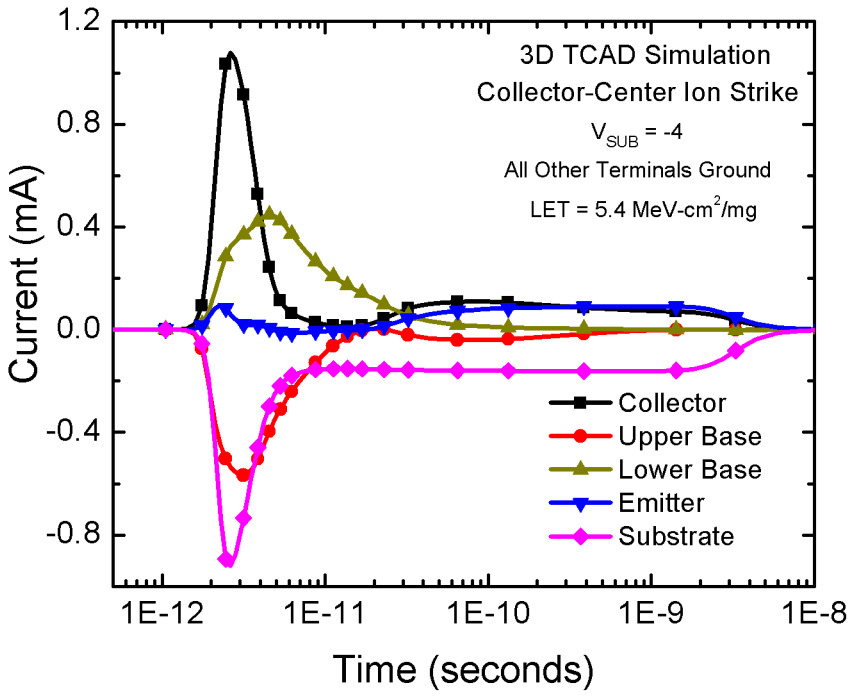


Figure 69: Simulated current transients for every device terminal of an inverse-mode cascode SiGe HBT as a result of an ion strike to the center of the collecter while subjected to bias scheme 1.

the explanation for this result provided previously is correct. The electrical collector shows two distinct shapes in the transient waveform. These include the current due to the deposition of charge directly within the depletion region of the collector-base substrate (the initial peak), and the current resulting from charge migrating from the subcollector to the collector terminal (the current plateau). Given the smaller impedance to cross the upper base-subcollector junction, the majority of electrons will diffuse across this junction.

The second ion strike simulation that was performed used the same device and strike location, but incorporated bias scheme 1. The simulated output current waveforms for all device terminals is shown in Figure 69 and the resulting integrated charge profiles is shown in Figure 70.

Once again, excellent agreement between experimental data and simulation data is

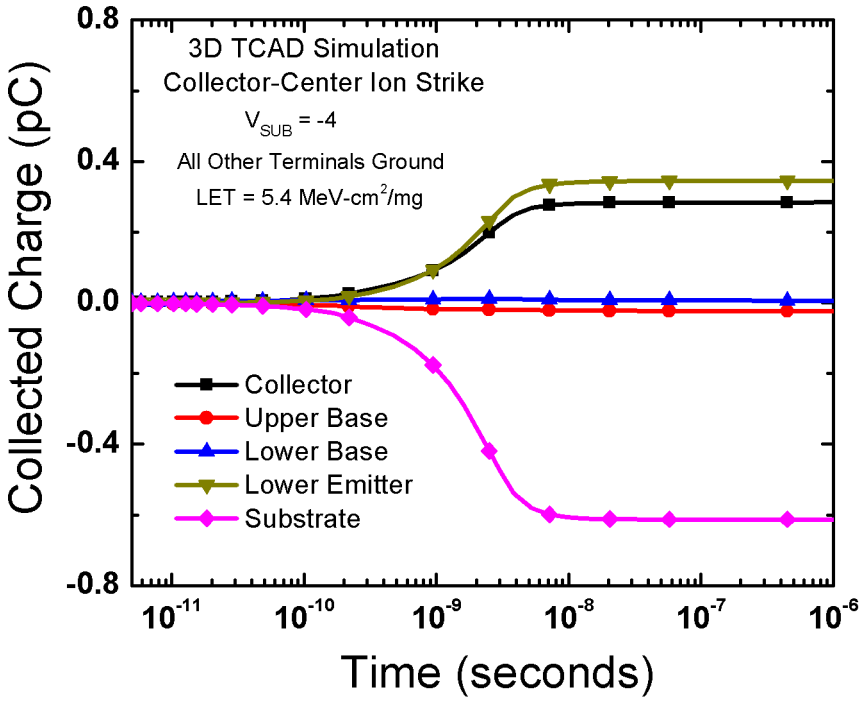


Figure 70: Integrated collected charge for every device terminal of an inverse-mode cascode SiGe HBT as a result of an ion strike to the center of the collecter while subjected to bias scheme 1.

observed (not for absolute charge collection values, but for the physical response of the device). In the current waveforms of Figure 69, several interesting points emerge. The first is that at very short times (¡10^{-11} seconds) the emitter terminal shows very small perturbations in the current (voltage). Similarly, the collector terminal has a very large spike in transient current. These observations are resulting from the choice of strike ion strike location (center of the electrical collector). Since no charge is directly deposited in the emitter-lower base junction, there will not be a large perturbation as seen for the collector terminal. The second piece of information that can be extracted is that the original interpretation of the experimental charge collection data, namely reduction of charge collection on the collector terminal arising from charge sharing between the emitter and collector terminals, is supported. As illustrated in Figure 69, both the electrical collector and emitter have current "plateau tails," of equivalent magnitude. When this current is integrated, it results in an equivalent amount of

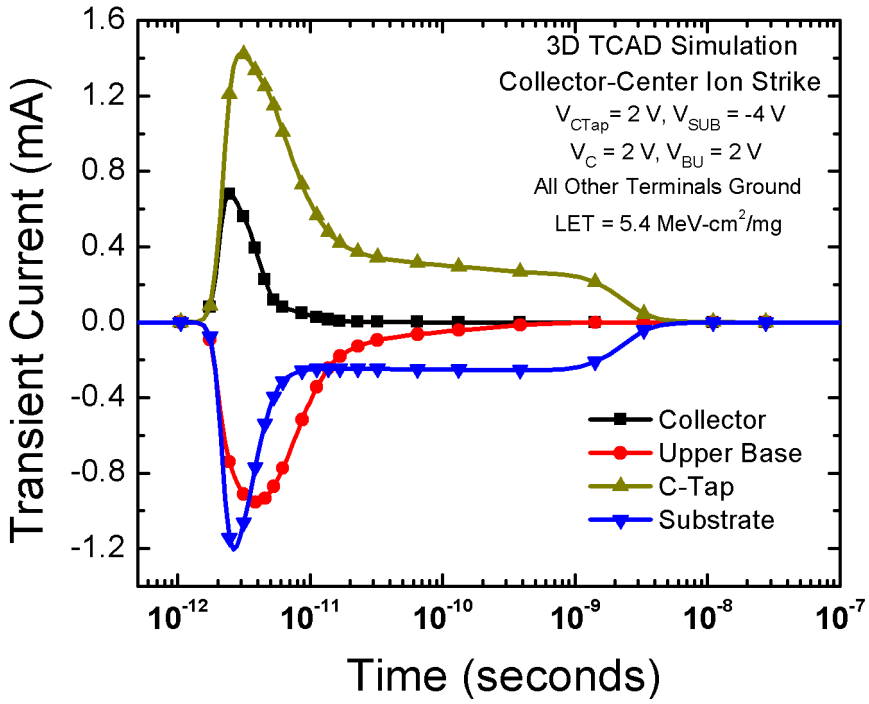


Figure 71: Simulated current transients for every device terminal of an inverse-mode cascode SiGe HBT with C-Tap as a result of an ion strike to the center of the collecter while subjected to bias scheme 2.

charge on both terminals, as illustrated in Figure 70.

Finally, the inverse-mode cascode SiGe HBT incorporating a biased C-Tap terminal was also simulated for an ion strike scenario. The location of the C-Tap terminal is depicted in Figure 66, and provides an electrical contact to the buried subcollector. The resulting current transient waveforms for all terminal and integrated charge profiles are shown in Figure 71 and Figure 72 respectively.

Once again the simulations are a reflection of the measurement results obtained. As can been seen in Figure 71, the presence of a C-Tap with applied bias results in nearly all electrons exiting through the C-Tap terminal. The only charge with is induced on the electrical collector terminal is due to the charge deposited directly within the depletion of the collector-upper base terminal. This is reflected in the collector current waveform of Figure 71, which shows only non-zero current directly following the ion strike event. Charges which are collected by the subcollector-substrate junction

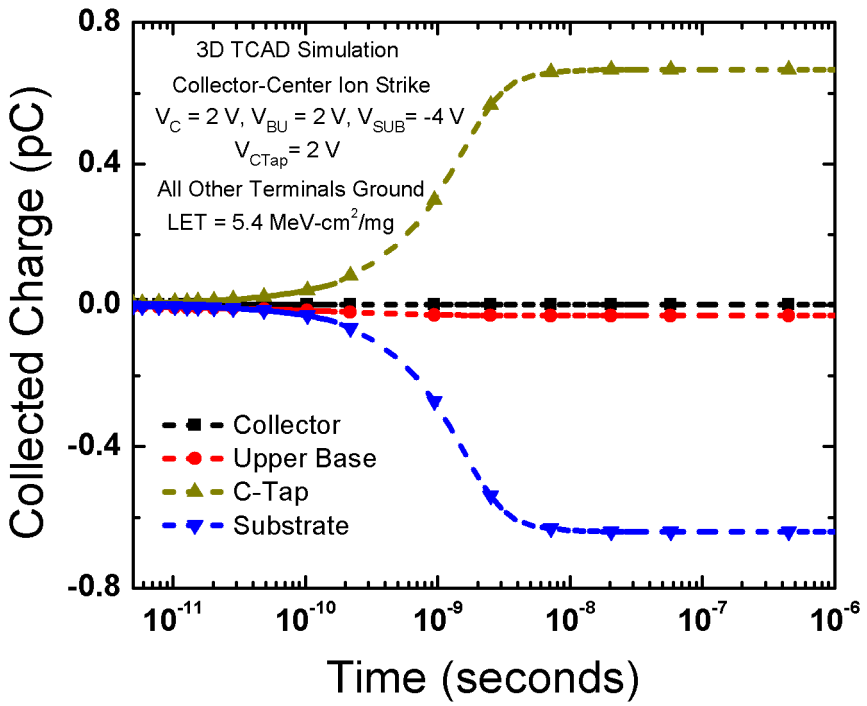


Figure 72: Integrated collected charge for every device terminal of an inverse-mode cascode SiGe HBT with C-Tap as a result of an ion strike to the center of the collecter while subjected to bias scheme 2.

are able to be effectively removed by the C-Tap terminal. This result suggests that by having a conductive electrical path out of the buried subcollector will provide significant SEU mitigation; however, complications arise considering how to effectively do this without comprising the operation of the inverse-mode cascode SiGe HBT.

5.3 Circuit-Level Radiation Sensitivity

5.3.1 Biasing the C-Tap Terminal

It has been shown that incorporating an electrical contact to the buried subcollector of the inverse-mode cascode SiGe HBT has the potential to offer incredible improvement in charge collection (SEU susceptibility) characteristics of the novel device. This conductive path from the buried subcollector to a rail is not a simple fix. The potential on the subcollector node changes dynamically in nominal circuit operation, adjusting itself to correctly bias the upper transistor (Q2) of the cascode, based on

the current state of the lower transistor (Q1). Recall that transistor Q2 essentially acts as a unity-current gain amplifier, where the input is the buried subcollector (the output of transistor Q1); therefore, the subcollector cannot be directly tied to a DC bias, as the bias point needs to dynamically change during device operation. Several concepts were developed to address this C-Tap bias concern, including a dynamically controlled FET conduction path to a rail and capacitive coupling to a rail. Given the simplicity of using a capacitor to tie the buried subcollector node to a rail voltage, this method has been investigated as a possible solution.

In order to theoretically verify the approach, Spectre simulations were employed. To represent the inverse-mode cascode structure with a subcollector node capacitively coupled to a rail, the schematic in Figure 73 was implemented. The HBT devices used were two discrete standard structures, with transistor Q2 operated in inverse-mode and transistor Q1 operated in forward mode. This allowed the device models in the Spectre environment to be utilized, given that the novel device has no operational models associated with it. To simulate the effects of capacitive coupling on the transient current waveform at the output node (Collector 2), a current source was tied to

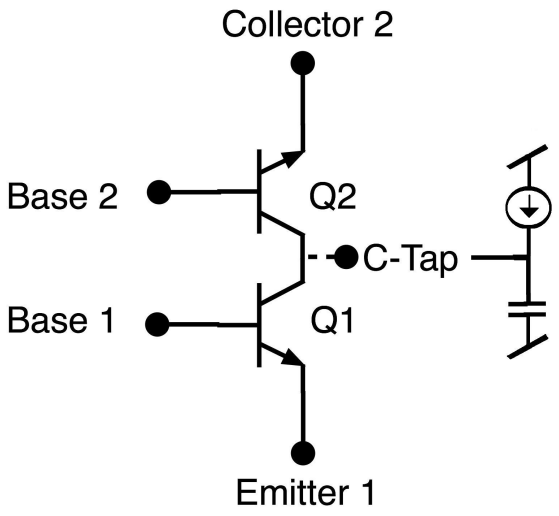


Figure 73: Schematic of the inverse-mode cascode SiGe HBT with capacitive coupling on the buried substrate. Transient current waveforms were injected on the subcollector terminal and measured at the output node.

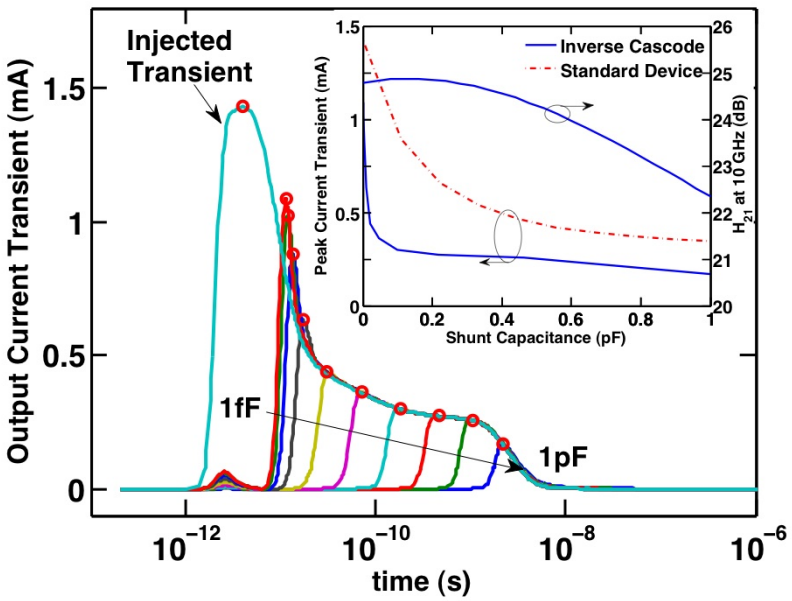


Figure 74: Simulated current transients on the output terminal for varying capacitor values on the buried subcollector node.

the subcollector node of the cascoded pair. This current source was programmed to inject the C-Tap transient current waveform that was generated using the ion strike simulation in NanoTCAD from Figure 71. A transient simulation was then executed in spectre with the cascoded pair operated in the "off" state (the previously defined bias scheme 2). Multiple simulations were run with varying capacitor values, the results of these simulations are presented in Figure 74. As evidenced by the simulations, capacitive coupling serves as an effective means of eliminating the current transient from reaching the output terminal. The mitigation of output current transients increases with an increase in the capacitor value (understood as lower frequency components become filtered with larger capacitor values). The maximum speed of a CML digital cell is expected to drop as the capacitor increases in size, so a trade-off exists between system speed and amount of SEU mitigation acquired.

5.3.2 Heavy-Ion Broadbeam Measurements

In order to guage the circuit-level impact of the IMC device in a radiation context, a full 16-bit master-slave architecture shift register was constructed with the IMC device using IBM's 3rd generation 8HP platform [101]. The IMC device design included a 100 fF capacitor attached from the C-Tap terminal to the high-voltage rail to provide partial decoupling of the subcollector-substrate junction from the device output terminal. A 16-bit master-slave shift register built with a cascode device topology was also fabriacated in the same SiGe BiCMOS technology. To provide a control circuit for comparison, a third variant, a standard non-cascoded 16-bit shift register, All three circuits were tested in air in a heavy-ion broadbeam environment at the Texas A&M Cyclotron Institute. The circuits were exposed to 15 MeV/u Neon, Argon, Xenon, and Krypton, and 25 MeV/u Nitrogen to provide sufficient range of linear energy transfer (LET) rates from 0.885 to 56.2 MeV-cm^2/mg. All three registers were operated at 500 Mbps while in the beam line and the total error count and ion fluence were recorded for each run to allow calculate of the error-cross section.

The calculated error cross-section for all three shift register variants are plotted in Figure 75. Both the standard cascode and the IMC shift register topolgies have larger error-cross sections for LETs greater than 10 MeV-cm^2/mg as compared to the control circuit. The increase in the error cross-section is a directly related to the increase in sensitive area of the cascode and IMC topologies. The inclusion of a cascode architecture results in the need for additional level shifters internal to the master-slave latch to accomodate the extra V_{BE} drop required by the cascode toplogy. These level shifters contribute to the sensitive area of the shift register as they are capable of generating upsets. Despite the increase in cross-section for moderate to high LETs, the low-LET performace of the IMC shift register reveals notable improvements in SEU. A zoomed-in picture of the low-LET statistics for all three shift registers is plotted in Figure 76. A clear improvement in the IMC error cross-section is evident

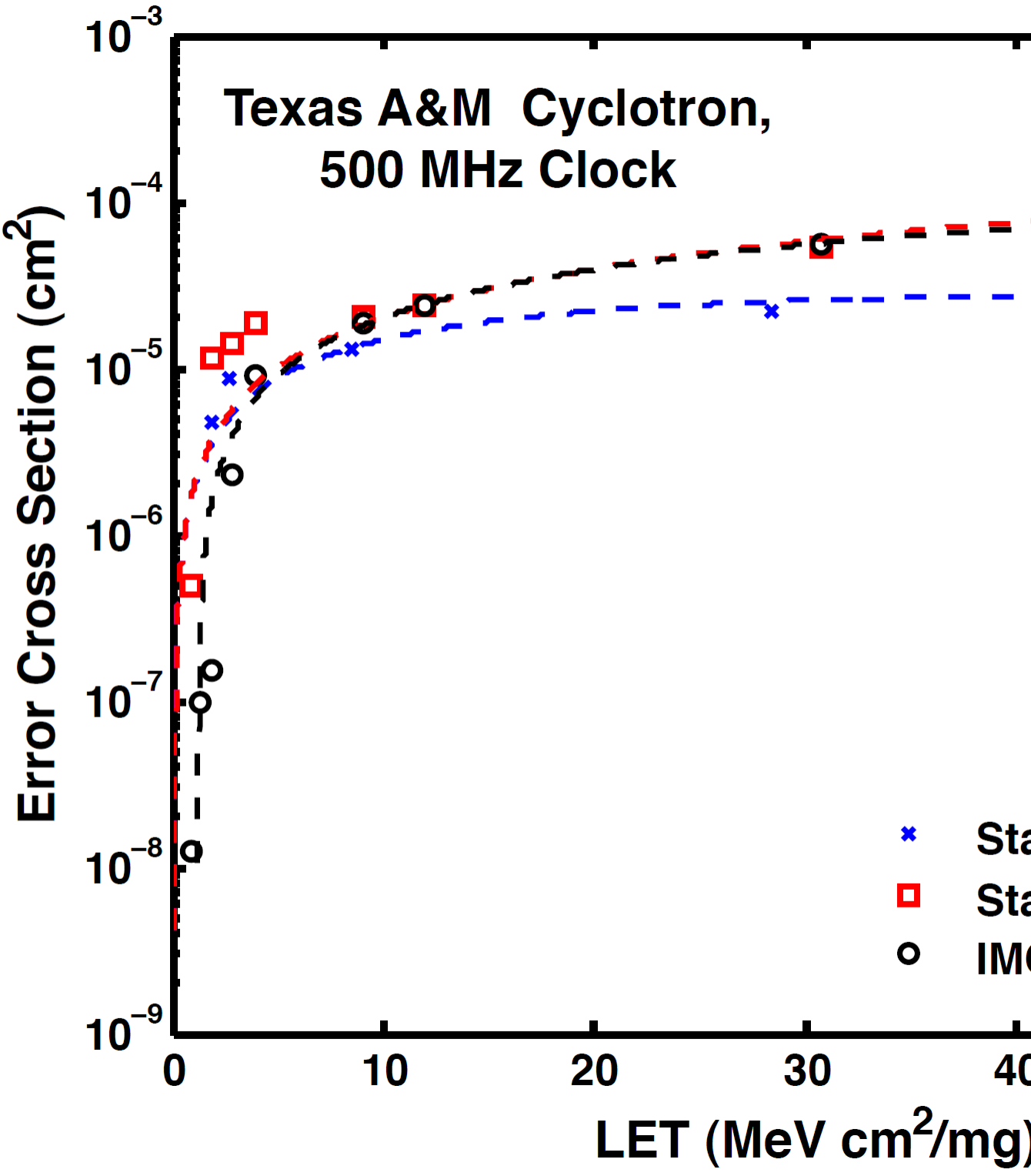


Figure 75: Measured heavy-ion broad-beam error cross section versus LET for standard npn,cascoded npn, and IMC shift registers.

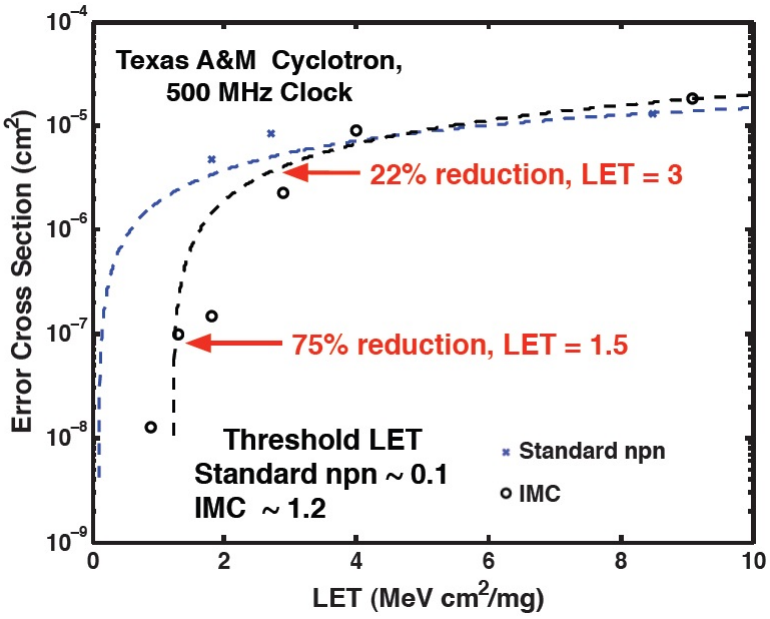


Figure 76: Zoomed error cross section versus LET for standard npn and IMC shift registers, highlighting the SEU hardening from the IMC devices at low LETs.

for low-LET values, with Weibull-fits showing a noticeable shift in the threshold LET of the latch. Given that the distribution of ion energy in the deep-space environment is heavily weighted for LETs less than 1 MeV-cm^2/mg, this improvement will have a large impact on the predicted system bit error rate.

CHAPTER VI

INVERSE-MODE OPERATION OF SIGE HBTS

6.1 Introduction

The most successful device-level radiation hardening by design (RHBD) technique (requiring no circuit redundancy) that has been developed in the the previous chapters, has been the inverse-mode cascode (IMC) SiGe HBT. This device architecture, when used to construct digital shift registers, is found to generate an improvement in SEU cross-section at low values of ion LET, at the expense of elevated saturated error-cross sections (a consequence of the additional internal level-shifters that increase the total sensitive volume of the circuit) [101]. This improvement in error mitigation has been attributed to the IMCs ability to decouple the output node of the lumped device from the sensitive subcollector-substrate junction in bulk platforms. An extensive study of the impact of the upper inverse-mode device on transient origination of the IMC has not yet been completed in the literature. Earlier 3D TCAD simulation work has postulated the performance of inverse-mode biased devices in a radiation context, but no experimental data has yet been available for support [4].

In the current chapter the single-event response of standard (non-cascoded) SiGe HBTs biased for inverse-mode operation (physical emitter biased as the electrical collector and vice-versa), in stand-alone devices and digital circuits is investigated, for the first time. Our intent is two-fold: 1) to assess the potential of inverse-mode operation of standard SiGe HBTs for possible SEU RHBD mitigation, and 2) to provide a deeper understanding of SEU mechanisms in SiGe HBTs. To accomplish these goals, heavy-ion broad beam measurements were performed on forward-mode and inverse-mode biased SiGe HBT digital shift registers in a silicon-on-insulator

(SOI) platform. The measured error cross-section curves are directly compared. Full 3-D TCAD simulations are used to provide a qualitative analysis of the results, and shed light on the underlying physical mechanisms of SiGe HBT ion-induced transient current origination that drive the differences between the forward and inverse-mode transient responses. To extend this learning to a bulk SiGe BiCMOS platform, stand-alone bulk SiGe HBTs were irradiated with a pulsed-laser, allowing direct capture of individual terminal transient currents. This experimental data is complemented with fully-coupled mixed-mode simulations that demonstrate the enhanced SEE mitigation of bulk inverse-mode SiGe HBTs.

6.1.1 Inverse-Mode SiGe HBTs

Simply stated, an inverse-mode SiGe HBT refers to the operation of a standard device with the collector and emitter terminals electrically swapped. The regime of inverse-mode operation has largely been viewed in the industry as a non-viable mode of operation, given the expectation of poor *dc* and *ac* performance. While it is true that inverse-mode performance suffers, resulting from inherently lower electrical emitter doping (a reduction in β) and a degraded base transit time from larger parasitics and larger base width (a reduction in f_T), it has been experimentally demonstrated that SiGe HBTs can be optimized for inverse-mode performance without process flow changes [3]. To illustrate this trade-off in performance, the simulated unity-gain cut-off frequency for a 1st generation SiGe HBT as a function of emitter current density is plotted in Figure 77. This simulation data was obtained with calibrated compact models from Texas Instrument's CBC8 technology process [5], where the nominal forward-mode biased SiGe HBT provides an f_T of 50 GHz. Continued technology scaling (vertical and horizontal scaling) has further boosted the performance of inverse-mode devices. Un-optimized inverse-mode devices from IBM's 3rd generation SiGe BiCMOS platform was shown to have an f_T of nearly 10 GHz in Chapter 5, while

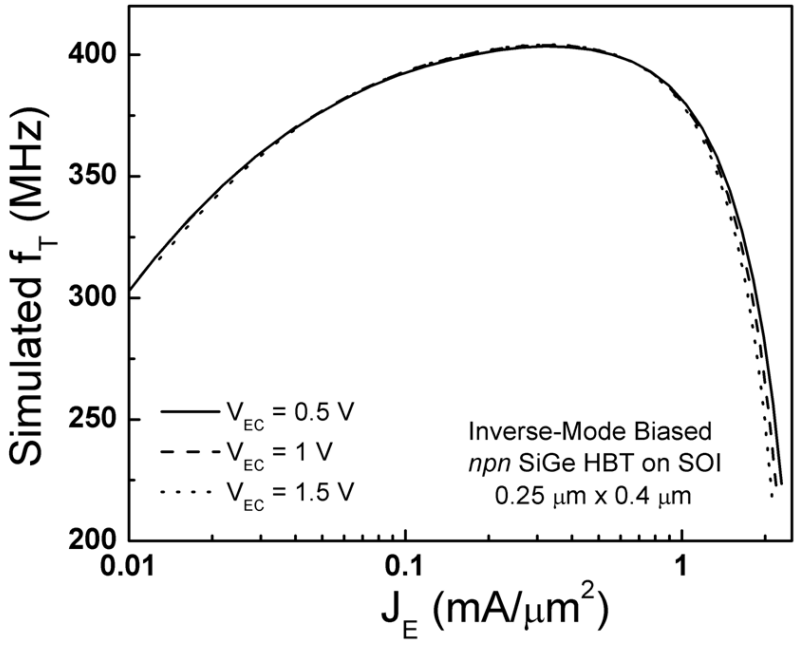


Figure 77: Simulated current transients for every device terminal of an inverse-mode cascode SiGe HBT with C-Tap as a result of an ion strike to the center of the collecter while subjected to bias scheme 2.

optimized inverse-mode devices from this technology process has been reported to have an f_T up to 20 GHz. More exotic alterations such as a tailored germanium profile in the base of the HBT can create built-in electric fields that further improve the ac metrics of the device. Future work is aimed at accomplishing this task.

It should be reinforced that the focus of this chapter is on stand-alone HBTs that are biased to operate in inverse-mode, which are not an IMC topology. As mentioned previously, the inclusion of IMC devices in circuit architectures, while out-performing stand-alone inverse-mode devices, results in shift registers with an increased number of gates compared to a forward-mode register of identical bit length. Instead of the IMC topology, a purely inverse-mode shift register allows a direct comparison to a forward-mode register, eliminating a variable from this already complex problem.

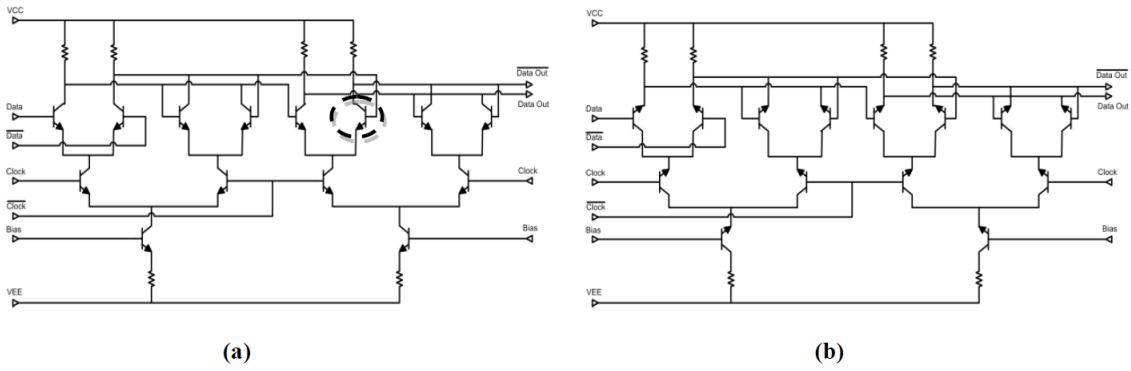


Figure 78: Schematic for the SiGe (a) forward-mode biased and (b) inverse-mode biased master/slave D flip-flop. The circled device in the forward-mode architecture was replaced with a full 3D TCAD model for mixed-mode simulations.

6.2 Experiment Details

6.2.1 Heavy-Ion Broadbeam

In order to explore the circuit-level SEE impact of inverse-mode operation, two 16-bit digital serial shift registers, built with a standard master/slave latch architecture, were fabricated using Texas Instruments CBC8 complementary SiGe BiCMOS technology platform. This 1st generation technology offers matched-performance *npn* and *pnp* HBTs with a peak f_T of 50 GHz, integrated on a thick-film SOI substrate. Previous heavy-ion experiments have illustrated the benefit of the SOI platform for mitigating SEU in digital shift registers [110]. Minimum sized (0.25 μm x 0.4 μm) *npn* SiGe HBTs were used to construct the forward-mode and inverse-mode latches. Transitioning from a standard forward-mode master-slave flip-flop architecture to an inverse-mode architecture is a simple process. Simplistically, the transition can be visualized by flipping all of the HBTs in a forward-mode design, as depicted in Figure 78. In addition to the inversion of the HBT, the bias current must also be adjusted to achieve the peak f_T of the inverse-mode biased device. This quiescent current is very similar to the forward-mode bias current, and only requires a small change in the tail resistance of the current mirror.

Both the inverse-mode and forward-mode shift register incorporated a gated-feedback cell clock tree, composed of devices biased in the mode of operation to match the joining flip-flop (forward or inverse-mode). The input and output buffers for both shift registers were constructed with forward-mode devices (to maximize the circuit output swing). The devices under test were packaged with high-speed custom-designed (PCBs) that were developed at the Mayo Foundation. The packages were brought to LBNLs BASE facility and irradiated with a 10 MeV/u and 16 MeV/u cocktail, both while in vacuum. The shift registers were measured at normal incidence for the 10 MeV/u cocktail, and at normal incidence, fifteen degrees, and thirty degrees for the 16 MeV/u cocktail. Both registers were monitored in-beam with an Agilent MP1764 BERT analyzer utilizing a 127-bit pseudo-random input data sequence. The DUTs were biased identically, maintaining similar input/output swings of 300 mV. The operating frequency of the registers was limited to 250 Mbps by the performance on the inverse-mode devices. As illustrated in Figure 77, the peak f_T for an un-optimized first generation inverse-mode device is only $\approx$ 400 MHz, over two decades lower than a forward mode device from the same technology process. Employing the optimization techniques of [3] will allow shift register circuits to be fabricated that operate in the Gbps range; speeds that satisfy the performance requirements of many orbital applications. Moving to highly-scaled (3^{rd} generation and beyond) technologies, where an un-optimized performances reach 200 GHz and beyond, will further enable the application of inverse-mode operation in moderate-frequency digital and RF applications.

6.2.2 Pulsed-Laser

Ideally, the SOI shift register broadbeam data would be directly compared to variants in a bulk technology; however, given the lack of industry-supported compact models for inverse-mode operation in bulk platforms, a quickly constructed variant was not

available. As an alternative, single-device measurements using NRLs pulsed-laser two-photon absorption (TPA) technique were obtained for a bulk technology. The *npn* SiGe HBT was from IBMs new fourth generation 9HP process (peak f_T/f_{max} of 300 GHz) bulk platform. A 0.1 μm x 1 μm device was packaged in custom-designed high-speed PCBs with the bottom substrate exposed. In this system, device-level current transients are induced by injecting carriers using TPA from a sub-bandgap pulsed laser and are then recorded using high-bandwidth measurement equipment, including a Tektronix DPO71254 12.5 GHz, 50 GS/sec, real-time oscilloscope. The pulsed-laser was positioned such that carriers were generated through the most sensitive position of the HBT (the physical-emitter center). The two bias conditions explored were: (1) a collector voltage of 0.8 V with all other terminals grounded (forward-mode-like) and (2) an emitter voltage of 0.8 V and all other terminals grounded (inverse-mode-like).

6.3 Broadbeam Results and Analysis

The analysis of the SEE-impact of inverse-mode operation will begin with a review of the heavy-ion broadbeam results that were obtained. Collapsing the data into the familiar error cross-section curves, the vital metrics (threshold LET, saturated error cross-section) can be easily extracted for both the forward and inverse-mode shift register architectures. The measured error cross-sections for both the forward and inverse-mode shift register are plotted in Figure 79 and Figure 80. This data is assembled from two separate broad beam experiments using two separate beam cocktails (10 MeV/u and 16 MeV/u) to maximize the statistics and verify the repeatability of the experiment. The normal incidence data is assembled from data from both ion cocktails and is plotted in Figure 79. A Weibull curve-fit was performed on these data points and is overlaid with the normal incidence data of Figure 79. The angled data (taken at 15° and 30°) was acquired with only the 16 MeV/u ion cocktail and is plotted in Figure 80 with the Weibull curves generated from the normal incidence

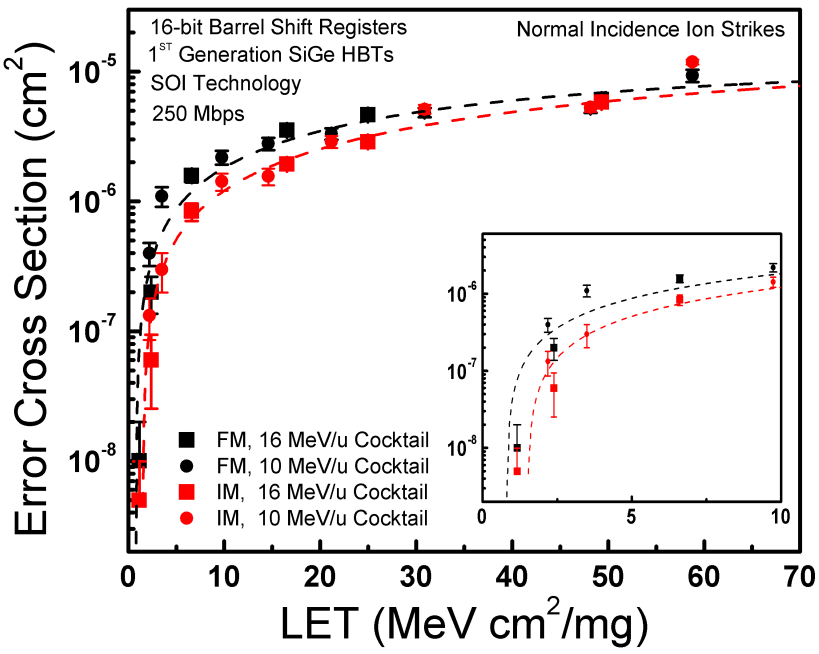


Figure 79: Measured bit-error cross-section curves for the 16-bit forward-mode and inverse-mode registers as a function of LET irradiated at normal incidence. The inset plot gives a zoomed-in picture of the low-LET data.

data-set overlaid once again.

Overall good agreement with the Weibull curve and angled data points are found for both shift registers; however, low-LET angled exposures experience more variability in the error-cross section for both register architectures. Reminiscent to previous measurements of the IMC shift register, the inverse-mode register achieves improved low-LET performance as compared to the forward-mode transistor. For LETs ranging from 0 - 25 MeV-cm^2/mg, the inverse-mode shift register error cross-section is reduced between 30 - 70% of the forward-mode cross section. Additionally, at LETs greater than 50 MeV-cm^2/mg, the two curves begin to converge, unlike for the IMC register that grows larger than the standard master/slave shift register beyond an LET of 10 MeV-cm^2/mg. From the fitted Weibull curve of the measured data, the threshold LETs for the forward-mode and inverse-mode register is extracted as 0.8 MeV-cm^2/mg and 1.5 MeV-cm^2/mg, respectively. This low-frequency result is expected to be consistent with higher frequency operation (for optimized inverse-mode circuits). As

the operating frequency is scaled, the window between clock-edge transitions decreases, increasing the probability of latched errors.

To estimate the potential system-level benefits of the inverse-mode shift register the CRME-MC tool [94] for SEE rate prediction was used to determine the reduction in errors for a typical satellite mission in geostationary orbit. Three different orbital environment scenarios were selected, spanning best to worst case scenarios for heavy-ion fluences. Error rates are determined given a predicted distribution of particles passing through 100 mil of aluminum shielding and the Weibull fit parameters from the measured broad-beam data. Identical RPP volumes were selected for the forward and inverse-mode shift register, as the sensitive volume for the SOI devices is primarily isolated to the intrinsic vertical stack of the emitter-base-collector junctions. Fully coupled mixed-mode simulations of this SOI technology were performed for the forward-mode architecture to verify that outside emitter strikes do not contribute upsets for moderate LET ion strikes. For grazing angle and very large LETs, substantial charge

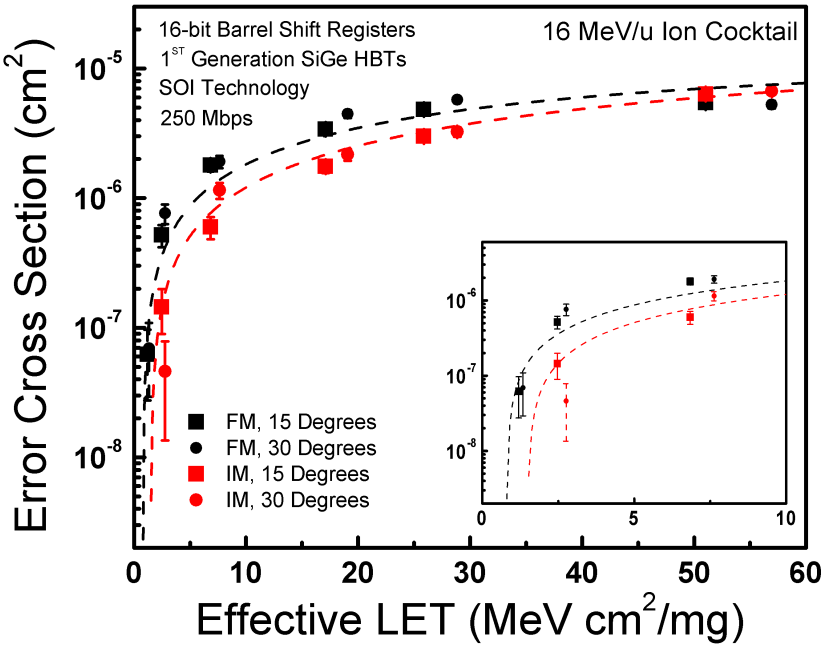


Figure 80: Measured bit-error cross-section curves for the 16-bit forward-mode and inverse-mode registers irradiated at two angles as a function of effective LET. The inset plot gives a zoomed-in picture of the low-LET data.

	Errors/ bit / day[1]		Reduction in Errors
	Forward-Mode SOI	Inverse-Mode SOI	
Solar Min	8.60E-09	2.43E-09	72%
Solar Max	1.33E-09	3.13E-10	76%
Worst Day	6.90E-06	2.28E-06	67%

[1] with 100 mil of Al Shielding

Figure 81: Comparison of bit-error rate predictions for the forward-mode and inverse-mode shift register architectures subject to three separate environment models.

can perturb the depletion regions to result in ion-shunting and possible latched upset (this does not occur for the inverse-mode architecture). As such, the matched RPP volume of the presented study is a worst-case scenario when comparing the forward and inverse-mode shift register predicted error-rates. Figure 81 highlights the reduction in errors for three orbital scenarios of the inverse-mode shift register over the standard forward-mode shift register. For solar minimum and maximum models, the inverse-mode shift register exhibits over 70% reduction in bit errors per day.

These positive results are, quite frankly, surprising considering that the inverse-mode register was fabricated with an SOI platform. Classically, it has been understood that inverse-mode operation would decouple the sensitive terminal of an HBT in a master-slave latch (the electrical collector) from the sensitive subcollector-substrate junction. For SOI processes, however, the substrate has been isolated from the device through the inclusion of the buried oxide, thereby inherently eliminating this sensitivity. For deeper insight into the error cross-section mitigation of the inverse-mode register, the difference in the total bit errors and the measured error intervals is plotted in Figure 82. This metric describes the number of bits in error that are counted within a single measurement interval of the BERT, and are a reasonable indication of the

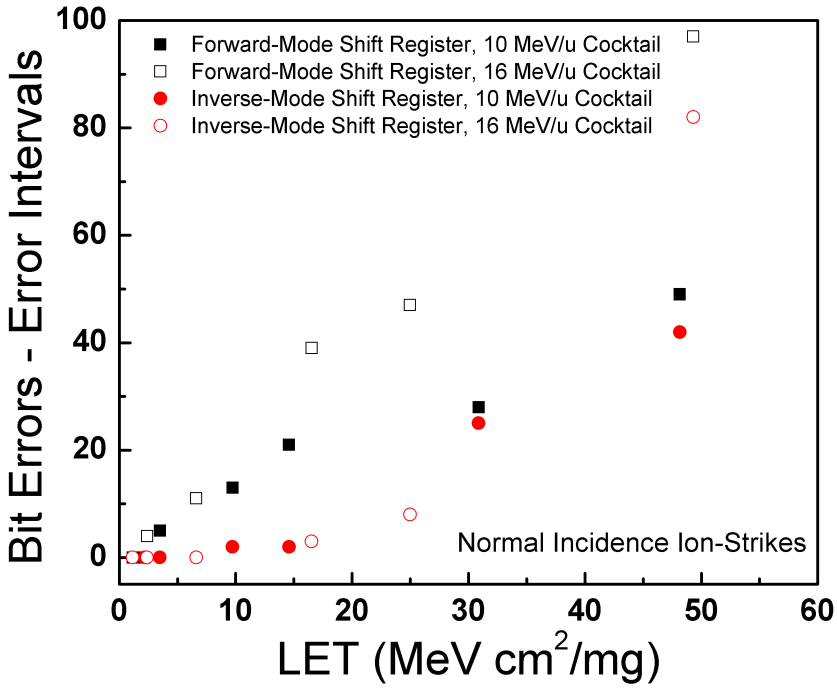


Figure 82: Difference in total bit errors and the number of bit intervals measured by the Anritsu MP1764 for the forward and inverse-mode shift registers as a function of LET.

magnitude of the combined multiple-bit-upsets (MBUs) and clock-tree-induced upsets. A clear trend that emerges from Figure 82 is that the inverse-mode shift register primarily experiences single upsets for LETs less than 10 MeV-cm^2/mg. Given the extremely low operating frequency of the two shift registers (250 Mbps) it is highly improbable that these multiple errors per interval are a result of multiple-bit-upsets (MBUs). Marshall et al., have previously measured the average number of MBUs at varying data rate for a first generation bulk master/slave shift register in [58], finding only single bit errors at data rates of 250 Mbps. This suggests that the SEU sensitivity of inverse-mode clock tree is improved compared to the forward-mode clock tree.

6.4 3D TCAD Modeling

For a more in-depth analysis of the heavy-ion broadbeam results, full 3D TCAD simulations were employed using CFDRCs NanoTCAD software package.

6.4.1 SOI Simulations

Built upon the framework of Spectre compact model simulations, a 3D model deck in NanoTCAD was developed for a 0.25 μm x 0.4 μm CBC8 *npn* HBT calibrated to both forward and inverse-mode dc characteristics. With this deck, the origination of ion-induced current transients was first investigated using physical-emitter-center strikes (a worst-case strike) for ion LETs varying from 0.5 MeV-cm2/mg to 60 MeV-cm2/mg. The strike position remains identical for both forward and inverse-mode biases (despite the electrical swapping of emitter and collector terminals), as the ion-passage through all stacked vertical junctions remains the most sensitive strike location. The modeled device was biased identical to an off-state CML device, the sensitive state for latch upset; here, the collector is at 3.300 V, the emitter at 2.465 V, and the base at 2.900 V for a forward-mode device. For an inverse-mode device the collector and emitter voltages were swapped. Previous mixed-mode simulations of Gbps SiGe shift registers have verified the electrical collector transient as the driving mechanism for latch upset [68]; therefore, our analysis will focus primarily on this transient terminal current.

The simulated electrical collector transient currents for the forward-mode (physical collector) and inverse-mode (physical emitter) biased device across multiple ion LETs are shown in Figure 83 and Figure 84, respectively. These figures can be delineated into two regions of the transient waveform, referred to here as Regions 1 and 2. Region 1 results from the collapse of the energy bands of the semiconductor after it is flooded with charge carriers. This effect has been described in the literature as the "ion-shunt" effect and was developed in Chapter 2. The collapse of the reverse-biased electrical collector-base depletion region results in a push-out, as field lines extend across the base, connecting the electrical emitter and collector terminals, a large current begins to flow from separated charges deposited from the ion strike in addition to injected electrons from the electrical emitter. Over time, the concentration of free charge carriers will drop as the electric field lines separate electron-hole pairs and remove

them from the active area of the intrinsic device. Once the carrier concentration drops below the doping level of the lower-doped side of the depletion regions (base), the emitter-base and collector-base depletion regions will reform, sustaining the full applied reverse voltage and removing electric field lines from the active region. The re-establishment of the electric field lines marks the onset of Region 2, where the remaining ion-deposited charges are separated by the depletion regions of the emitter-base and the collector-base junctions. The transient current for this region originates from the passage of the remaining ionized free carrier concentration flowing through the electric-field lines of the reestablished depletion regions. The presence of a "knee" region in the inverse-mode biased device is a consequence of the higher carrier concentrations present in the active area of the intrinsic device following the collapse of the ion-induced shunt. With the reduction in duration of the shunt region for the inverse-mode bias, less charge is separated from the electric field lines that are established from the shunt itself. This effect intensifies at higher LET, as seen in Figure 84.

Although the initial collapse of the electrical emitter-base junction is identical for both biases, the electrical collector-base junction dynamics are significantly different and this drives the disparity between the two transient responses. Figure 85 and Figure 86 show the vertical electric field component along a 1D cut through the emitter center of the 3D model for both bias conditions. Initially the electrical emitter-base and electrical collector-base junctions can be easily identified; however, following the ion strike the field lines almost entirely disappear. However, the strong electric field in the electrical collector-base junction however is not completely neutralized. When comparing the forward and inverse-mode devices, the strength of the field lines is significantly different after the strike. The insets of Figure 85 and Figure 86 provide a closer look at the field levels around the electrical collector-base junction for each bias condition. The larger doping levels present in the electrical collector-base

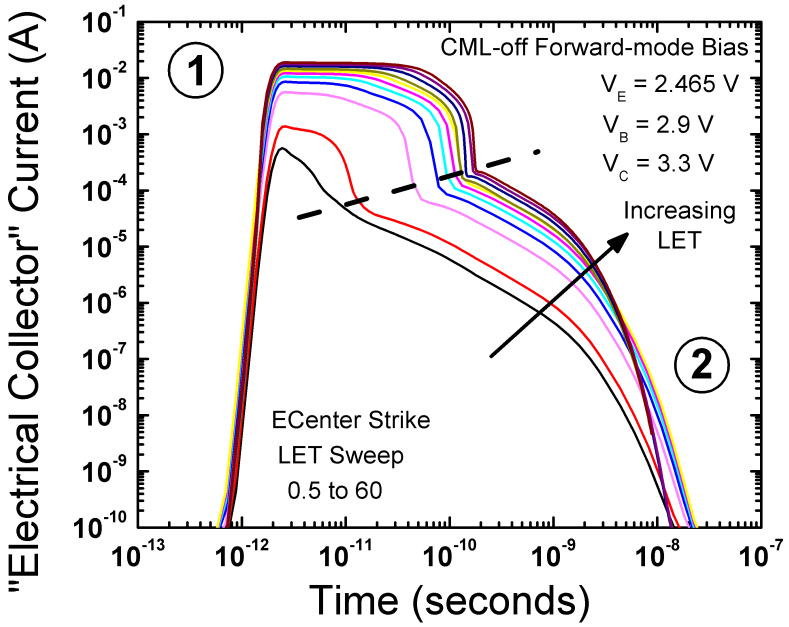


Figure 83: Simulated electrical collector (physical collector) transients for a modeled SOI 1st generation SiGe HBT biased in the forward-mode configuration. Multiple ion LET have been simulated, covering values from 0.5 to 60 MeV-cm^2/mg.

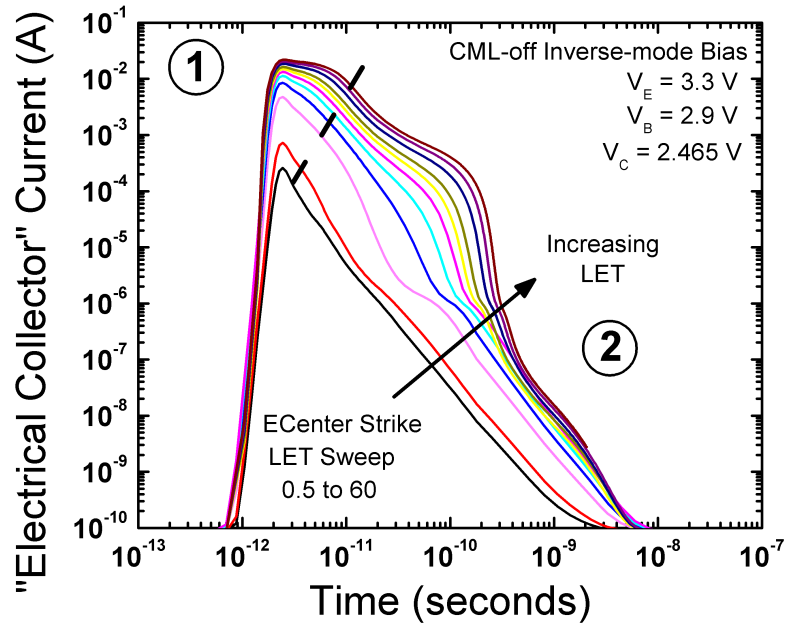


Figure 84: Simulated electrical collector (physical collector) transients for a modeled SOI 1st generation SiGe HBT biased in the inverse-mode configuration. Multiple ion LET have been simulated, covering values from 0.5 to 60 MeV-cm^2/mg.

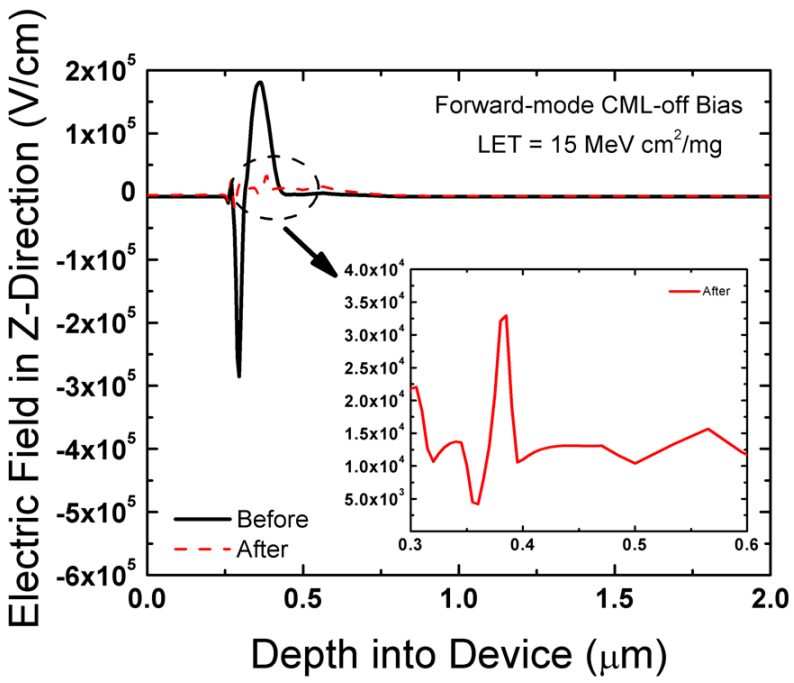


Figure 85: Simulated vertical electric field lines through the center of a first generation SiGe HBT in an SOI process, biased for forward-mode operation, before an ion strike and directly following an ion strike.

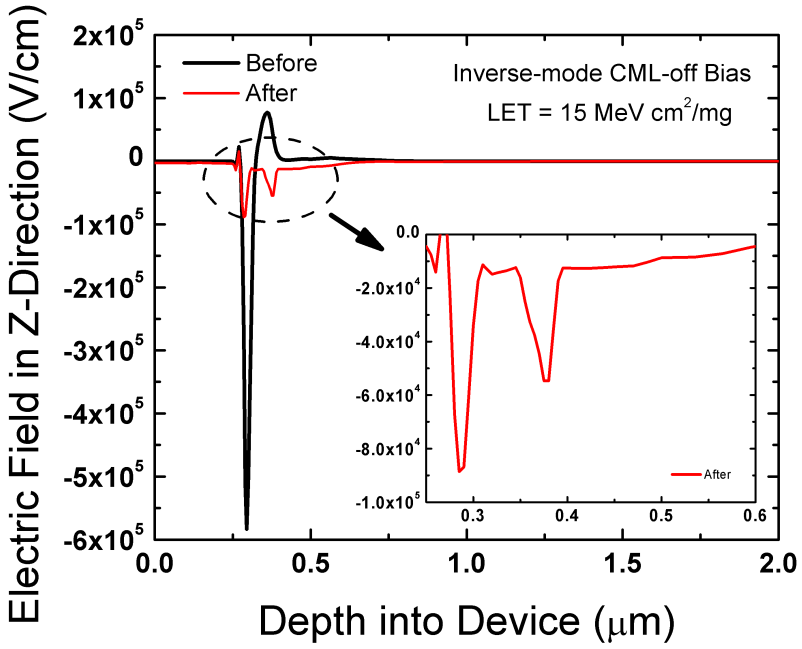


Figure 86: Simulated vertical electric field lines through the center of a first generation SiGe HBT in an SOI process, biased for inverse-mode operation, before an ion strike and directly following an ion strike.

junction for the inverse-mode case (physical emitter-base junction) result in much larger initial electric field lines that are not as easily neutralized as the lower doped electrical collector-base junction for the forward-mode bias. These larger fields after the strike result in elevated drift current levels that more quickly reduce the excess carrier concentration in the base of the transistor, which in turn more quickly shuts off the high-current shunt mechanism once free carrier concentrations drop below the high-doping concentrations in the electrical base-emitter doping.

The reduction in the shunt duration of the inverse-mode biased device has important implications for understanding SEE in digital shift registers and drawing conclusions for other applications. For digital shift registers, certain devices in the master/slave architecture are sensitive only to upsets that occur on a clock edge. A reduction in the high-current shunt duration results in a decreased probability of upsets being clocked into a latch. While this does not alter the threshold LET of the latch, it does reduce the cross-section across all ion LETs. This is directly illustrated in the error cross-section data of Figure 79 and Figure 80. As inverse-mode operation is improved through optimization schemes and operating frequencies increase, this effect will become more pronounced (assuming that the optimization schemes do not dramatically alter the origination of ion-induced transient currents). For applications that are charge-sensitive (e.g., VCOs [23]), inverse-mode biases result in nearly an order of magnitude lower charge being induced on the electrical collector terminal as illustrated in Figure 87, once again resulting from a reduction in the duration of the ion-shunt. Although these results are positive, it does bring to light an apparent trade-off between device breakdown voltage and SEE performance, as elevated doping levels and large, confined electrical fields can undermine device reliability.

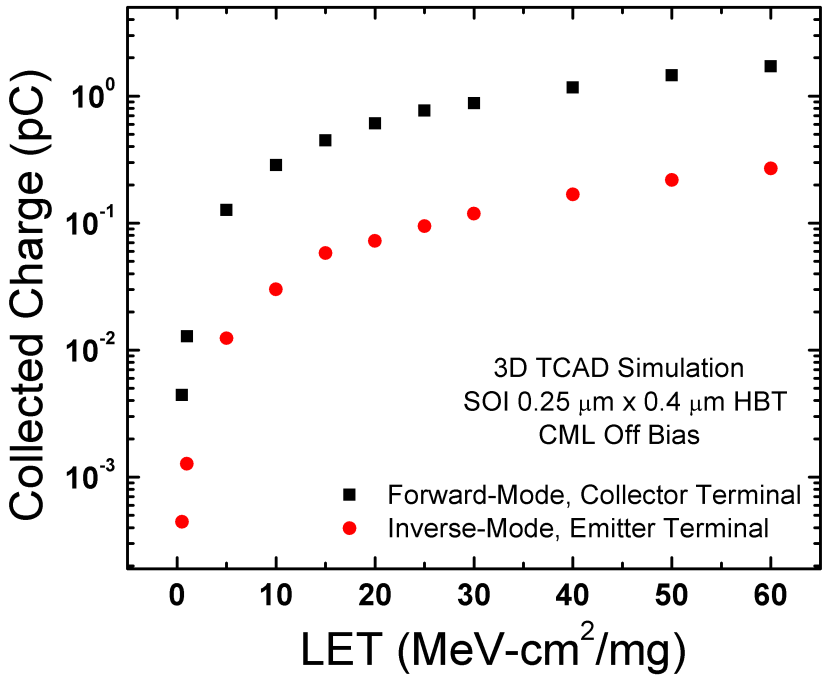


Figure 87: Simulated total collected charge on the electrical collector terminal for both the CML-Off forward-mode and inverse-mode bias.

6.4.2 Bulk Simulations

The analysis of transient origination of inverse-mode biased devices was extended by simulating an emitter-center strike in a similar first generation bulk SiGe platform. A moderate LET value of 7 MeV-cm^2/mg was selected and a comparable inverse-mode CML-off bias was chosen. The transient currents induced on all device terminals are plotted in Figure 88. Once again the waveform can be delineated by the two regions, as described previously. The presence of the ion-shunt is evident as the electrical collector and emitter have similar magnitudes but opposite polarities during that period. The physical collector also demonstrates the characteristic diffusion tail that arises from charge carriers being separated by the subcollector-substrate junction. As expected, the electrical collector (physical) emitter terminal of the inverse-mode device is isolated from this current path.

To demonstrate the added sensitivity that the diffusion tail provides, fully-coupled mixed-mode simulations were performed. The forward-mode master/slave architecture

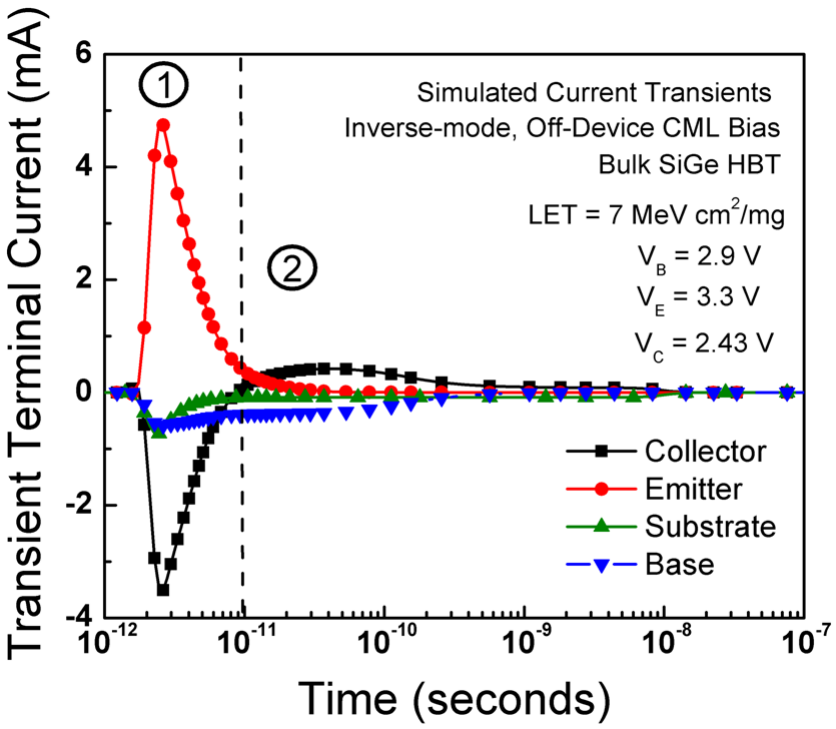


Figure 88: Simulated transient currents for a bulk 1st generation SiGe HBT biased for a CML-off state. Separation of the ion-induced shunt regime and standard junction charge collection is identified.

of Figure 78 was used, with a 3D TCAD device replacing the slave input device circled in the schematic. For this simulation, the ion path was set to be centered on the collector terminal, such that no charge is generated within the intrinsic device and only through the subcollector and substrate. The static bias prior to ion strike is as follows: V_{CC} = -5.2 V, V_{EE} = 0 V, V_{Data} = -0.3 V, $V_{Databar}$ = 0 V, V_{Clock} = -0.8 V, $V_{Clockbar}$ = -1.2 V and V_{Bias} = -3 V. The clock edge transition resulting in latching the slave input state to the storage cell (-1.2 V to -0.8 V) was varied over a range of 900 ps, while the ion strike time was held constant at 2 ps. This allowed us to determine the duration of sensitivity of the device for bit upset. The data inputs were held at fixed biases, such that the normal clock transition should not result in a transition of the output state. Figure 89 plots the voltage transients of the output of the latch for all simulated clock transitions and clearly demonstrates the sensitivity of forward-mode latch upset to

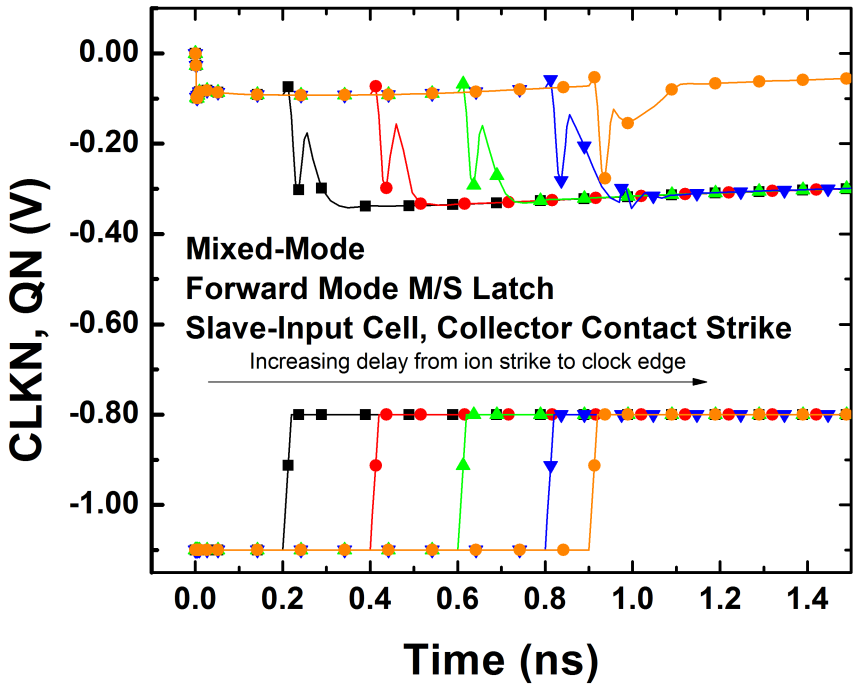


Figure 89: Mixed-mode voltage transients for ion strikes to the slave input off device with increasing delay to the clock edge. The strike time is held constant 2 ps.

ion strikes external to the emitter. This has exciting implications for inverse-mode architecture in a bulk technology, as the electrical collector terminal has been shown in calibrated simulation to be isolated from the transient current originating from the subcollector-substrate junction. This will effectively confine the sensitive area of the device to be closer to the area of the selectively implanted collector as opposed to the deep trench area, for normal incidence ion strikes. For a minimum-sized HBT in IBMs first generation 5AM bulk SiGe technology platform, this results in a 76% reduction in sensitive area. This reduction in sensitive area will couple forward to a global reduction in the error cross-section of the measured inverse-mode bulk shift register.

6.5 Pulsed-Laser Results and Analysis

The purpose of the final measurements using NRLs backside laser TPA measurement system was to experimentally validate the simulated transient profiles. Upon arrival to

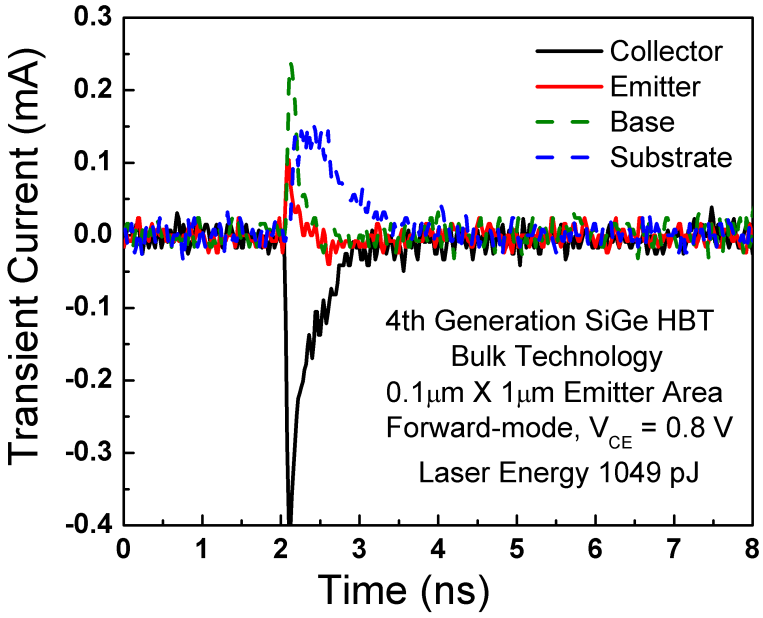


Figure 90: Laser-induced measured transient currents on all terminals of a minimum sized, 9HP bulk device with a forward-mode bias of 0.8 V on the collector.

the facility it was discovered that the backside substrate surface of the bulk hardware was of extremely poor quality, leading to some scattering at the backside interface and therefore uncertainty in the exact energy deposition within the SiGe HBT. However, as this data is only meant for qualitative comparison purposes, and all comparisons are performed for the *same* device on the *same* substrate, the exact metrics for energy deposition are not required.

Figure 90 and Figure 91 illustrate the measured laser-induced transient currents on all device terminals for a forward-mode-like bias of 0.8 V on the physical collector and for an inverse-mode-like bias of 0.8 V on the physical emitter of the device. Figure 92 directly compares the electrical collector transient currents for the forward and inverse-mode biased device. As expected from simulation, the polarity of the emitter and the collector transient currents are swapped for forward and inverse-mode biases during the ion-shunt region. Looking closely at Figure 91, the first sampled point of the physical collector transient has a positive polarity, followed by a change in the sign of the collector current. The ion-shunt duration lasts for a very brief period of time

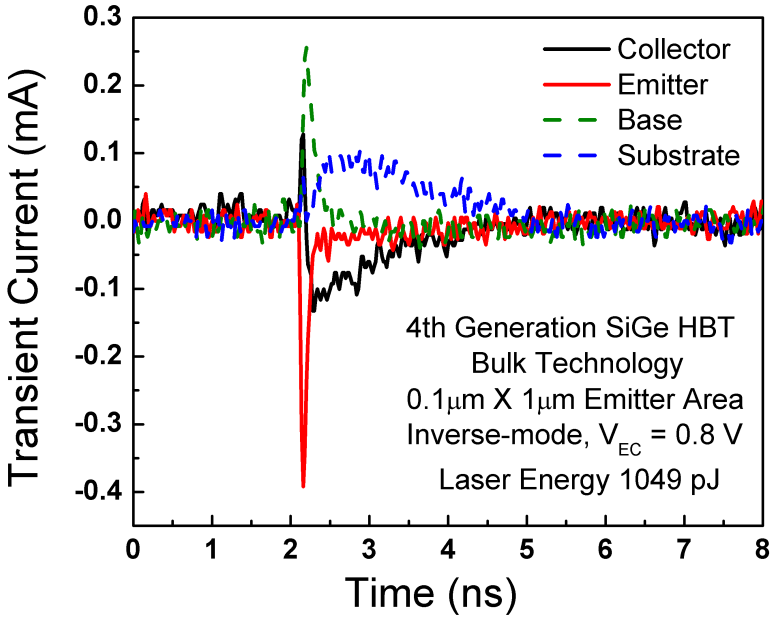


Figure 91: Laser-induced measured transient currents on all terminals of a minimum sized, 9HP bulk device with an invere-mode bias of 0.8 V on the collector.

for inverse-mode biases, as illustrated in Figure 84. For a very high LET of 60 MeV-cm^2/mg, the shunt lasts for only approximately 20 ps. (As the sampling oscilloscope is limited to 20 ps/sample, it is understandable that only a single sampled point of the ion-shunt region can be captured experimentally for the inverse-mode biased device.) The collector transient current following the collapse on the shunt in Figure 91 arises from the separation of electrons from the collector-base and subcollector-substrate junctions.

The direct comparison of electrical collector transient currents in Figure 92 reveals another experimental validation of the simulation data. By integrating the terminal currents it is found that approximately 131 fC of charge is induced for the forward-mode bias, whereas only 56 fC of charge is induced for the inverse-mode bias. The physical emitter terminal of the inverse-mode biased device in Figure 92 also clearly illustrates the effective isolation of the emitter terminal transient from the subcollector-substrate junction induced transient current, when observing the full-width half-maximum (FWHM) of both bias conditions. The FWHM extracted from the electrical collector

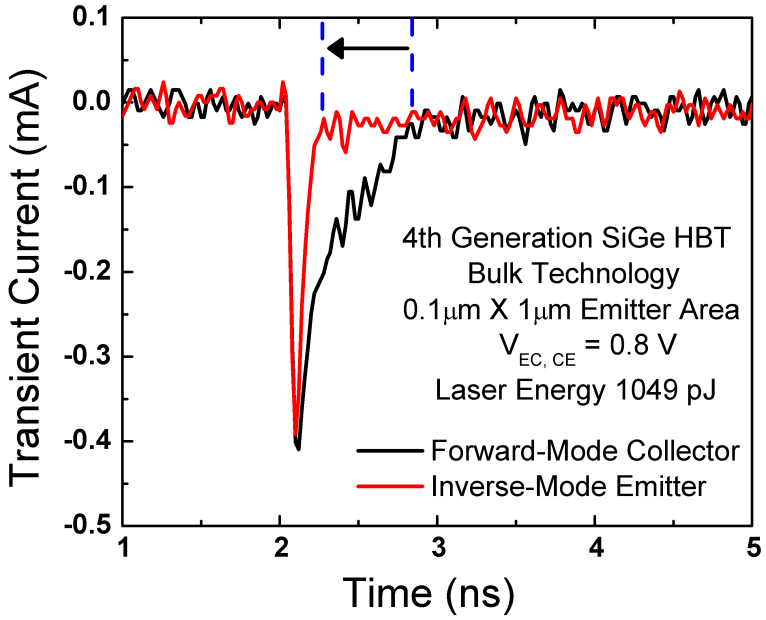


Figure 92: Comparison of electrical collector laser-induced measured transient currents for the forward and inverse-mode bias of the 9HP SiGe HBT. Attention is drawn to the reduction in transient duration for the inverse-mode device biased device.

transient signals of both the inverse-mode bias and the forward-mode bias is 0.05 ns and 0.21 ns, respectively. As previously demonstrated with mixed-mode simulations of the latch architecture, this will lead to significant reductions in the sensitive area of the HBT, and, as such, the error cross-section curve.

6.6 Conclusions

It has been shown experimentally, for the first time, the impact of inverse-mode device operation on the origination of ion-induced transient currents for both bulk and SOI SiGe BiCMOS technology platforms. With a combination of heavy-ion broadbeam measurements on digital shift registers and fully-coupled mixed-mode TCAD simulations, the enhanced error mitigation associated with inverse-mode operation in both bulk and SOI SiGe BiCMOS technology platforms has also been demonstrated. Although un-optimized inverse-mode operation offers reduced device performance and remains unfeasible for many applications, steps have been outlined for improving inverse-mode performance. Optimization techniques will enhance the performance metrics of this

mode of operation, increasing the feasibility of incorporation into charge-sensitive, Gbps applications, such as shift registers, low-noise amplifiers, and voltage-controlled oscillators. The low-frequency trend in improvement of the inverse-mode architecture is expected to be maintained as the system frequency is scaled down. Transient origination remains identical, regardless of circuit operating frequency. As the circuit frequency increases, the probability of a clock transition occurring during the sensitive window of the transient waveform (ion-shunt and subcollector-substrate funnel) increases. With the reduction in shunt-duration of the inverse-mode architecture, the ratio in error reduction between the two architectures should be maintained as the frequency is increased. As the operating frequency increases beyond the duration of the sensitive window of the transient current for the forward-mode biased device, the presence of multiple-bit upsets (MBUs) in forward-mode architectures could further improve the response of the inverse-mode register.

When considering optimization of devices intended for inverse-mode applications, it is important to consider the impacts of these techniques on the origination of ion-induced transient currents. It is highly probable that device modifications to enhance inverse-mode operation will alter the ion-induced transient characteristics, especially if doping levels of the electrical collector-base junction are altered; however, the isolation of the subcollector-substrate junction for bulk platforms will prove to be a suitable trade-off for this optimization. By eliminating the sensitivity introduced by the subcollector-substrate junction, inverse-mode devices behave identically to SOI devices with regard to SEE except without the high-cost of using an SOI platform [110]. This bulk behavior could prove to be a large gain in the radiation tolerance of systems destined for orbital applications, despite the losses in system performance.

CHAPTER VII

SINGLE EVENT EFFECTS IN MIXED-SIGNAL SIGE HBT CIRCUITS

To this point, the impact of ion-induced transient currents in SiGe HBTs has focused on specific simple, digital applications. These applications have had clearly defined, discreet digital states for input and output signals, simplifying the characterization and quantization of transient-induced events. An ion-induced upset is easily distinguishable and measured when sampled binary state transitions are the only variable of concern. It has been shown that calculating the event cross-section provides a suitable means of extrapolating the system-level error rates for these systems, as the frequency of digital state upset remains the dominating effect in ascertaining system sensitivity. This metric for quantifying SEE sensitivity is not complete, however, for analog and mixed-signal applications. Mixed-signal systems incorporate transitions between multiple signal domains (analog/RF to digital, and vice-versa). Analog and RF signals are inherently variable in nature, encompassing a potentially complex combination of magnitudes and durations for a fixed system. Establishing error criteria for these applications in non-trivial, as the impact of multiple variables must be described to adequately assess downstream impacts. Traditional error-cross section data sets are often insufficient as stand-alone descriptions of single-event sensitivity for analog applications, as transient impacts are typically characterized by multiple variables (i.e., duration, magnitude, phase deviations). Establishing new figures of merit for single event reliability of mixed-signal systems and identifying effective ion-induced transient hardening methodologies is currently a hot area of research.

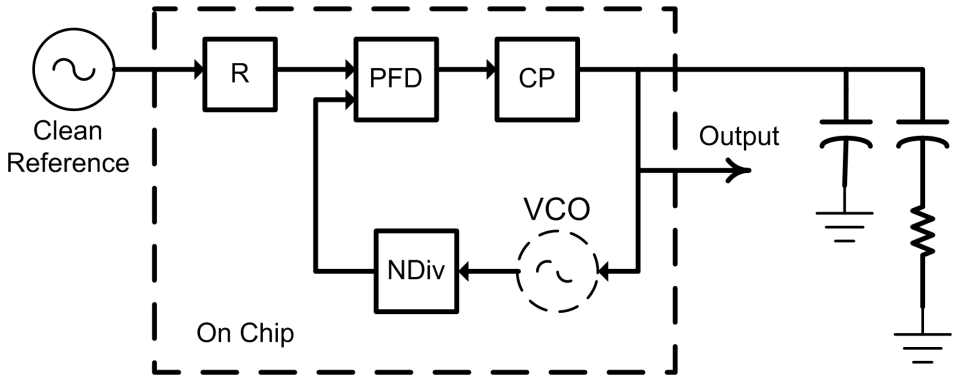


Figure 93: General block diagram of an Integer-N frequency synthesizer.

Phased-locked loops (PLLs) are ubiquitous components for terrestrial and space-based wireless communication systems. PLLs are incredibly versatile circuits that span the application space of clock recovery, clock skew reduction, data synchronization, frequency modulation and demodulation, and frequency synthesis [55]. The need for spectrally clean, programmable frequency sources remains paramount for translating information embedded in RF signals between the high-frequency carrier and baseband processing modules for any orbital mission. A block diagram of a simple integer-N frequency synthesizer is depicted in Figure 93. The fundamental operation of a PLL is linked to the generation of a stable output signal which is locked in phase to a reference input signal. For frequency synthesizers, the input reference is a spectrally clean source (crystal oscillator). This input is then passed through an initial frequency divider (R-Divider) to bring the input down to the comparison frequency. The phase-frequency detector (PFD) compares this input with the output signal of the feedback loop divider (N-divider). Phase differences in the two signals result in a voltage signal fed into the charge pump (CP), which translates the signal to a current. The loop filter impedance-transforms this current into a control voltage that tunes the frequency of the voltage-controlled oscillator. In this way, the divided output of the VCO is tuned to match the phase of the clean reference, which implies that the frequencies will be matched and the output frequency will be given by:

$$F_{out} = \frac{N}{R} * F_{in} \tag{7}$$

The block diagram of Figure 93 is only a single variant of many possible frequency synthesizer PLL architectures. The addition of an accumulator and a delta-sigma modulator in the feedback path give rise to a fractional-N PLL, which allows finer resolution frequency channels without the expense of smaller comparison frequencies and spurious noise sources closer in frequency to F_{out} [7]. The VCO, shown here on chip, is also often omitted as an integrated component for greater flexibility of commercially sold parts (customizable frequency range through incorporation of varying off-chip VCOs).

The impact of transient events on a multitude of digital-based PLLs has been performed by multiple investigators in previous years [56, 42, 54, 53, 52, 9]. These studies have spanned individual analysis of sub-block components (VCOs, dividers) as well as complete closed-loop system analysis. Loveless et al, have offered a thorough analysis of single event transient propagation in closed-loop PLL systems built upon the framework of linearized equations for the loop response [55]. This analysis highlights the importance of characterizing the phase displacement introduced by transient strikes that arise from individual sub-components of the PLL and draws important conclusions for design optimization for ion-induced transient mitigation of closed-loop PLL systems. This work was performed in a purely CMOS framework (encompassing 90 nm and 130 nm technology nodes); however, the general learning from the analysis can be extended to mixed-signal PLL systems from any technology family.

Silicon germanium BiCMOS technology is gaining momentum for incorporation into analog and RF applications given its competitive high-speed performance, low-noise metrics, and ease of integration with standard silicon CMOS processing [41]. Frequency synthesis applications and wireless communications in general stand to directly benefit from the inclusion of SiGe BiCMOS technology. These systems

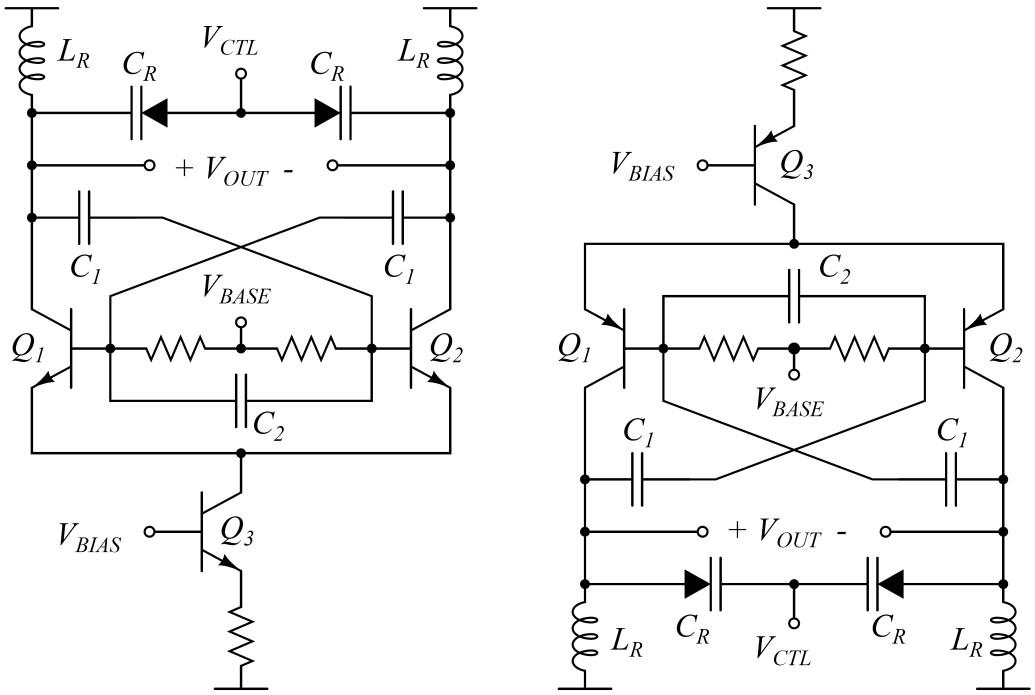
can leverage the high-performing HBT for critical components (high-speed dividers, LNAs, low-noise mixers and oscillators) while relying on low-power MOSFETs for the high density digital processing blocks. SiGe BiCMOS technology platforms are exceptionally attractive for mixed-signal systems destined for extreme environment, particularly those environments encompassing ambient radioactive particle fluxes. While tradition silicon MOSFETs are highly susceptible to ionizing damage from radioactive particles [24], SiGe HBTs have been experimentally demonstrated to be highly robust to permanent ionization effects. This resilience is a highly desirable trait for any system exposed to ionizing radiation, as lifetime reliability is dependent on minimizing excess leakage currents and shifts in dc operating points. Although SiGe HBTs greatly improve the total ionizing dose (TID) damage response, we have demonstrated in previous chapters that this technology is particularly susceptible to single event effects. As such, it is vital to analyze the impact of single-event transient currents that originate from sub-components of a PLL system that is constructed with SiGe HBTs.

The research presented in this chapter is focused on single-event transient effects arising from three particular sub-components of the closed-loop PLL illustrated in Figure 93. These components include the VCO, the integrated CP-PFD, and the frequency dividers (both R and programmable N divider). Our study will begin with an in-depth analysis of the origination of transient effects in cross-coupled resonant tank oscillator based VCOs. The theory developed from this work is not reserved for SiGe HBT-based VCOs, but can be extended to other technology platforms built with a resonant tank architecture. The second section looks into the impact of single-event transients on charge pumps constructed using SiGe HBTs. The transient response of programmable frequency dividers constructed from SiGe HBTs is presented in the final section of the chapter.

7.1 Single Event Transients in SiGe-Based Resonant Tank Oscillators

7.1.1 Single Event Transient Theory

Oscillator circuits are unique RF blocks, as they operate independent of external stimuli to generate a frequency tone from internal noise sources. The schematic for a resonant tank voltage-controlled oscillator constructed with *npn* SiGe HBTs and also with *pnp* SiGe HBTs is shown in Figure 94. The cross-coupled differential pair forms a negative resistance component (positive feedback amplifier) which serves to amplify the internal noise of the SiGe HBT. The passive impedance formed by the inductor and capacitive passive network forms a frequency selector which isolates the resonance of the amplifier to a fixed tone. The varactors serve as a tuning mechanism, allowing the total capacitance to be varied which in turn modulates the resonance frequency. In this way the oscillating frequency can be tuned linearly over a fixed



(a) *npn*-only (b) *pnp*-only

Figure 94: Schematic for an (a) *npn*-only and a (b) *pnp*-only reasonant tank oscillator.

range of control voltages. The output voltage of the LC tank VCO is given by the differential voltage across the capacitors which can be defined generally as

$$v_c(t) = A\cos\omega_0 t \tag{8}$$

where A is the equilibrium amplitude where the negative impedance of the active devices and resistive losses of the passive elements are balanced and ω_0 is the resonant frequency set by the LC network. A thorough derivation of the underlying equations giving rise to this general expression is outlined in [37].

Early investigations of resonant tank oscillators built from *npn* SiGe HBTs documented the measured transient characteristics of the oscillator output when subjected to a focused, pulsed laser [13]. This study unveiled modulations in both the instantaneous phase and amplitude of the oscillator and was able to successfully reproduce identical transient waveforms in a quasi 3D-TCAD platform. No detailed explanation was provided, however, for the underlying physics that gives rise to these laser-induced transient perturbations. As part of a collaborative effort, analytical expressions which explain both the modulations in phase and amplitude and predict signal perturbation from theory were derivated. Expanding (8) to incorporate the resulting transient-induced perturbations, we have the following equation:

$$v_c(t,t') = (A + \Delta A(t,t'))\cos(\omega_0 t + \Delta\phi(t,t')) \tag{9}$$

where t' is a time immediately following an ion or laser-strike event. To develop analytical expressions for $\Delta A(t,t')$ and $\Delta\phi(t,t')$, we must first build upon some fundamental assumptions. For brevity, the full analysis leading to these analytical expressions has been omitted. Interested readers are directed to where the full analysis is performed. It is the intent for this document to describe the assumptions that build this theory and give a qualitative description of the results.

When an energetic ion passes through a semiconductor system, a wake of free ionized charge is left in its wake. If collected by sensitive terminals of a SiGe HBT,

this charge can influence the output of the oscillator. Assuming that deposited charge is collected by the transistor in a timely fashion, the injected charge into the LC tank can be modeled as an ideal step, or a Dirac delta function. The inductor of the LC network will resist this sudden change in current, resulting in all charge being dropped on the capacitor. This sudden change in charge is translated to a change in frequency by the capacitance such that

$$\Delta v_{tran} = \frac{\Delta q}{C}. \tag{10}$$

This voltage step adds directly with that steady-state voltage across the capacitor, and given that this voltage is periodic, the superimposed characteristic will be dependent on the relative phase of the oscillator at the moment of the strike. The derivative of the voltage dropped across this capacitor will not change; however, as the derivative of the voltage step is the Dirac delta function, which is zero for all times except at the strike instant. The state change, as a result of charge injection, can be written as

$$v_c(t'^{+}) = v_c(t'^{-}) + \Delta v_{tran} \tag{11}$$

$$\dot{v_c}(t'^{+}) = \dot{v_c}(t'^{-}). \tag{12}$$

This response can be visualized by turning to a phase plane repreasentation of the steady-state operation of a resonant tank VCO, as shown in Figure 95. The time-dependent signal state can be represented by a two-dimensional vector, $\vec{S}$, which is a superposition of both $v_c(t)$ and $\dot{v_c}(t)$. For a fixed period of the oscillating waveform, this vector will form a complete path on the phase plane, which is known as the limit cycle of the oscillator. Figure 95 also demonstrates the impact of an ion-strike event on the vector $\vec{S}$. For this event two distinct effects are apparent, namely a change in phase and magnitude of $\vec{S}$. The dashed line in the figure illustrates the decay path as the oscillator returns to the limit cycle. This brand of transient event is labeled a "bulge" transient. A second type of transient event which can occur from the framework of this theory is a "dip" transient, where the perturbed vectors phase

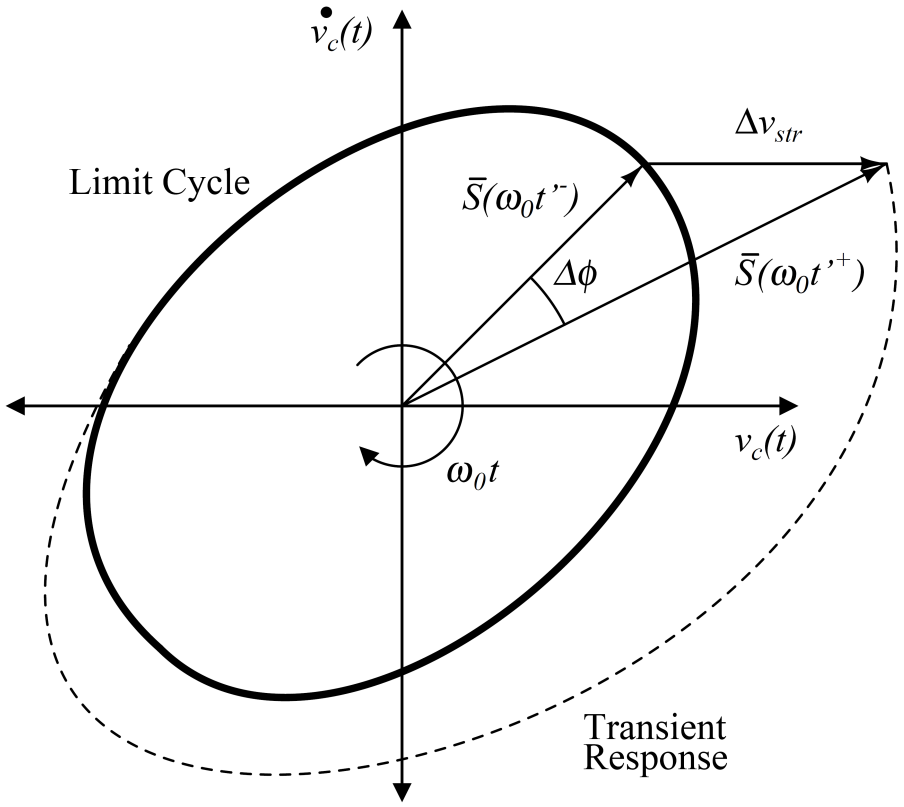


Figure 95: Phase plane visualization of the limit cycle of a resonant tank oscillator. An ion strike (occuring at time t'^+) will either push the oscillator into a new state within the limit cycle, or outside the limit cycle.

is changed but remains within the limit cycle of the oscillator. The exact transient event that occurs depends on both the magnitude of the collected charge as well as the relative phase of the oscillating signal at the time of the strike. This analysis has been built upon a similar argument formulated to explain noise phenomena in oscillators [32]. From the analysis of transient perturbations in resonant tank oscillators and the resulting expressions for $\Delta A(t, t')$ and $\Delta\phi(t, t')$ two important figures of merit can be defined and evaluated numerically. These FoM include the total phase displacement as defined previously in [56]. The second figure of merit is the total duration of the transient, determined once the perturbations in phase and magnitude settle within a set threshold level.

7.1.2 Experimental Validation

To evaluate the theory that has been discussed in the previous section, resonant tank VCOs were fabricated on a complementary SiGe:C BiCMOS process from IHP [35]. This technology offers a 90 GHz vertical *pnp* device combined with a matched 100 GHz *npn* mapped onto a 0.25 μm platform featuring a 200 GHz high-speed *npn*. Identical *npn* and *pnp* VCO architectures, shown previously in Figure 94, were fabricated to allow a direct comparison. The oscillators were designed to operate at a resonant frequency of 1.4 GHz. Custom-designed printed circuit boards (PCBs) were designed and fabricated using a high-speed compatible Rogers 4003c dielectric to maintain signal fidelity. Coplanar waveguide transmission lines were designed on the top layer metal to be matched to 50 ohms impedance at a peak frequency of 25 GHz. The silicon die were mounted over a clearance hole at the center of the board, such that the backside surface of the die was optically exposed, and wirebonded to the signal pads of the transmission lines of the top metal. In addition to the VCOs, stand-alone *npn* and *pnp* SiGe HBTs of matched emitter area (0.22 x 0.84 x 4 μm^2) to the HBTs used in the VCO design were mounted on separate PCBs with identical transmission lines. These devices were padded and wirebonded such that all device terminals were accessible during testing.

Both the packaged VCOs and the stand-alone devices were tested at the Naval Research Laboratorys pulsed-laser lab. The VCO circuits were irradiated on the backside substrate using the TPA measurement system described in Chapter 1, while the stand-alone device were irradiated on the top surface with the SPA measurement system. Time domain captures of instantaneous perturbations in oscillation frequency and laser-induced transient currents on stand-alone device terminals were acquired with a high-speed Tektronix DPO71254 real-time oscilloscope. This equipment has an analog bandwidth of 12.5 GHz, and allows 50 GS/s rates giving a timing resolution of 20 ps/point. It was discovered during the pulsed-laser testing that the both the

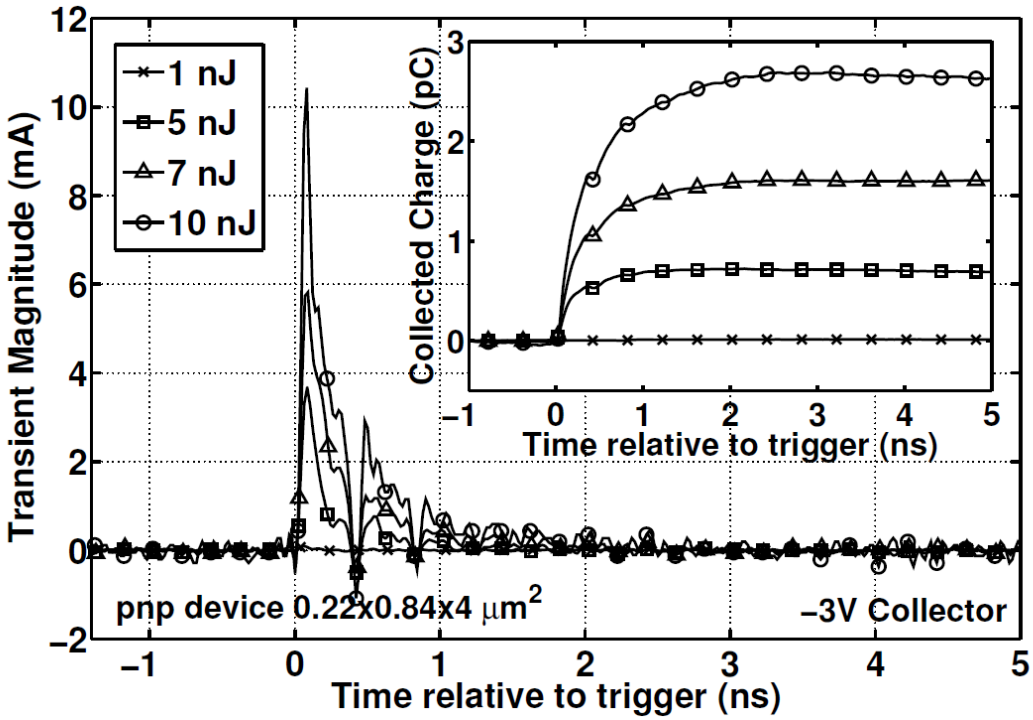


Figure 96: Transient current waveforms induced on the collector terminal of a *pnp* SiGe HBT for multiple laser energies. The inset shows the integrated charge for each energy.

npn based VCOs and stand-alone devices experienced catastrophic failures during irradiation. The *npn* SiGe HBTs essentially became resistively shorted between collector and emitter, eliminating all bipolar action. It was determined that this effect was an artifact of the laser measurement system and not indicative of real catastrophic failure events in a heavy-ion environment. Processing-induced trap states in the silicon bandgap of the *npn* SiGe HBTs result in an amplification of the induced charge carriers from the photon packets. This effect can essentially double or triple the deposited charge within the system leading to unrealistic levels of ionized charges. The failure mechanism was probabilistic in nature, allowing for small data sets on npn circuits to be collected before system failure; however, this data is identical to the *pnp* data, so only those results are shown here for brevity.

The induced transient currents on the collector terminal of the stand-alone *pnp*

SiGe HBT for multiple laser energies is shown in Figure 96. Only the collector terminal results are plotted, given that only the base and collector terminals contribute charge to the LC tank of the VCO. The induced base charge is several orders of magnitude lower than the collector, leaving the collector as the dominating terminal. As can be seen in Figure 96, the transient currents induced on the collector are reminiscent of transient signatures observed in SOI platforms, as they lack substantial long-duration tail currents. Although the IHP technology is a bulk technology, this platform offers triple-well isolation for the pnp devices. This triple well architecture mitigates the induced transient current by isolating the subcollector-substrate junction with an additional n-well. As such, this transient current can be modeled as a simple double exponential function, for the simulation purposes in the following discussion. Also shown in Figure 96, is the total integrated charge on the collector terminal for each laser energy. As this profile shows a characteristic of a "rounded" unit step function on a time scale similar to the oscillation frequency of the measured VCO, it is necessary to use an expanded analytical expression as documented in [37] to calculate the perturbations in phase and amplitude for these induced charges. This calculation allows us to generate some expected values for the previous described figures of merit (phase deviation and transient duration).

Scanning the pulsed-laser across the active area of the VCO circuit uncovered several regions of sensitivity. These included the cross-coupled differential pair of SiGe HBTs and the SiGe tail current source. It was found that directly striking the varactors did not result in any transient perturbations of the oscillating waveform. This is a surprising result as the varactors were simple bulk diode structures and were expected to contribute charge to the LC tank. Once the sensitive areas were established, the pulsed-laser was focused on the emitter-center of one of the cross-coupled SiGe HBTs, such that the developed theory could be validated. The laser energy was varied over the same range as the stand-alone devices, 1 nJ to 10 nJ, which was determined to

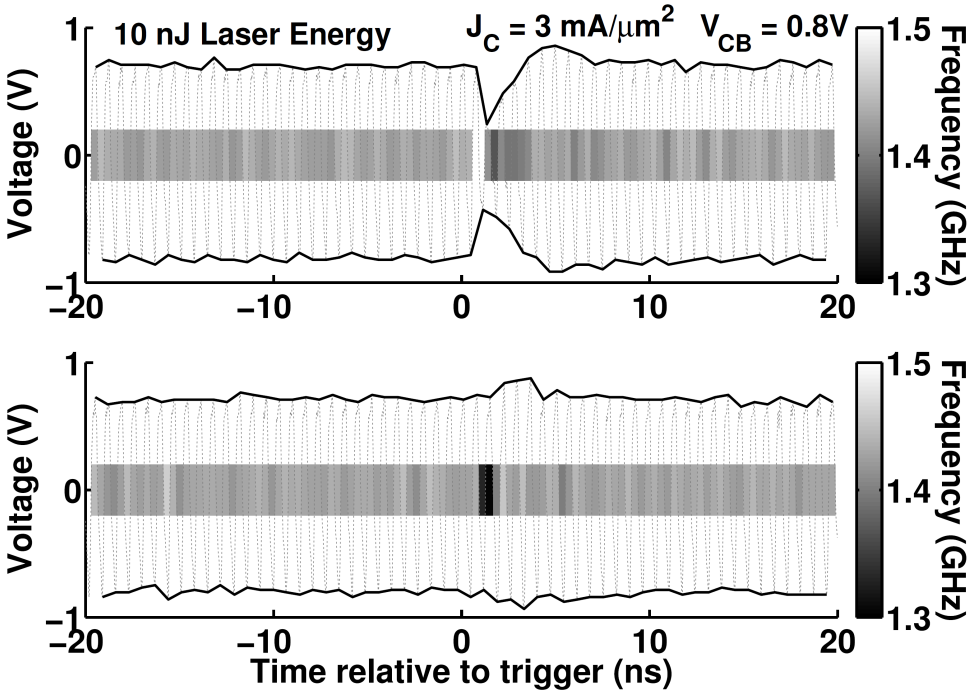


Figure 97: Two measured SETs of the *pnp*-only VCO design which cleary illustrate the "bulge" and "dip" type transients that were developed from theory. The intesity bar show the instantaneous frequency shifts (phase chage) for each SET.

give a maximum space-relevant LET of 100 MeV-cm^2/mg based on direct comparisons with SRAM cells [91]. Figure 97 plots two characteristic transient signatures which were consistently measured for all laser energies. For ease of analysis, the envelope of the two waveforms is plotted, in addition to the calculation of the instantaneous frequency, as determined by the time of zero-crossings of the waveform. These two waveforms illustrate the bulge and dip characteristic perturbations which were defined earlier from theory. Figure 97 also demonstrates the instantaneous phase shift that occurs following a transient event.

A third class of transient signatures was also measured that is not captured by the theory to date. This type of transient perturbation is illustrated in Figure 98, where the oscillation is essentially collapsed for a sustained duration before restarting. Earlier investigators have observed this type of perturbation, but have not offered

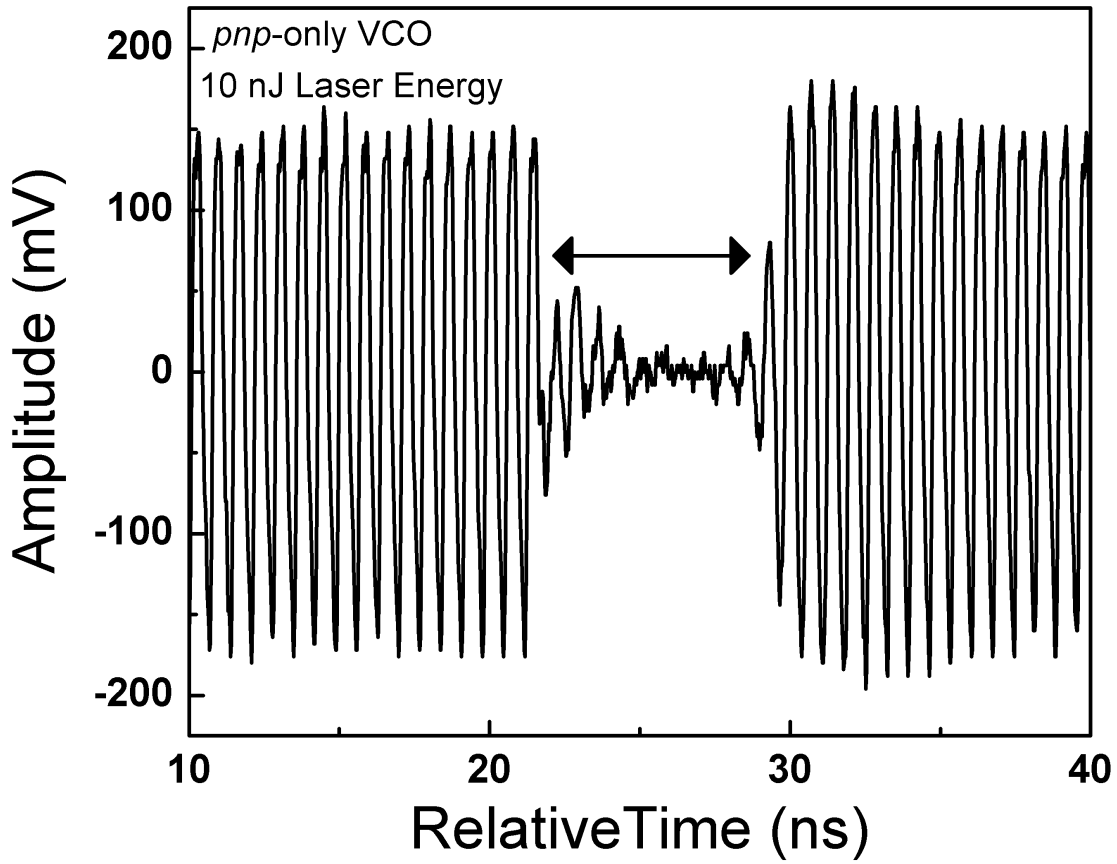


Figure 98: Worst-case measured SET of a *pnp*-only VCO design, where a sustained collapse of oscillating waveform occurs at large laser energy.

explanation for the occurrence [13, 51]. This type of transient event only occurred for the peak laser energy used, 10 nJ. To understand this event, it is necessary to first recall the underlying theory of resonant tank oscillators. In its simplest form, sustained oscillations are a delicate balance of the negative resistance supplied by the active SiGe HBTs and the resistive losses of the LC tank. The negative impedance of the HBT is a bias dependent quantity, normally evaluated when the HBT is operating in the forward-active mode. For large laser energies, the induced charge on the capacitor is sufficient to push the HBT in the breakdown, where the negative resistance is not sufficient to maintain oscillation.

The data that was collected from the pulsed-laser experiment can also be plotted by calculating the two figures of merit which have been defined previously. To perform this

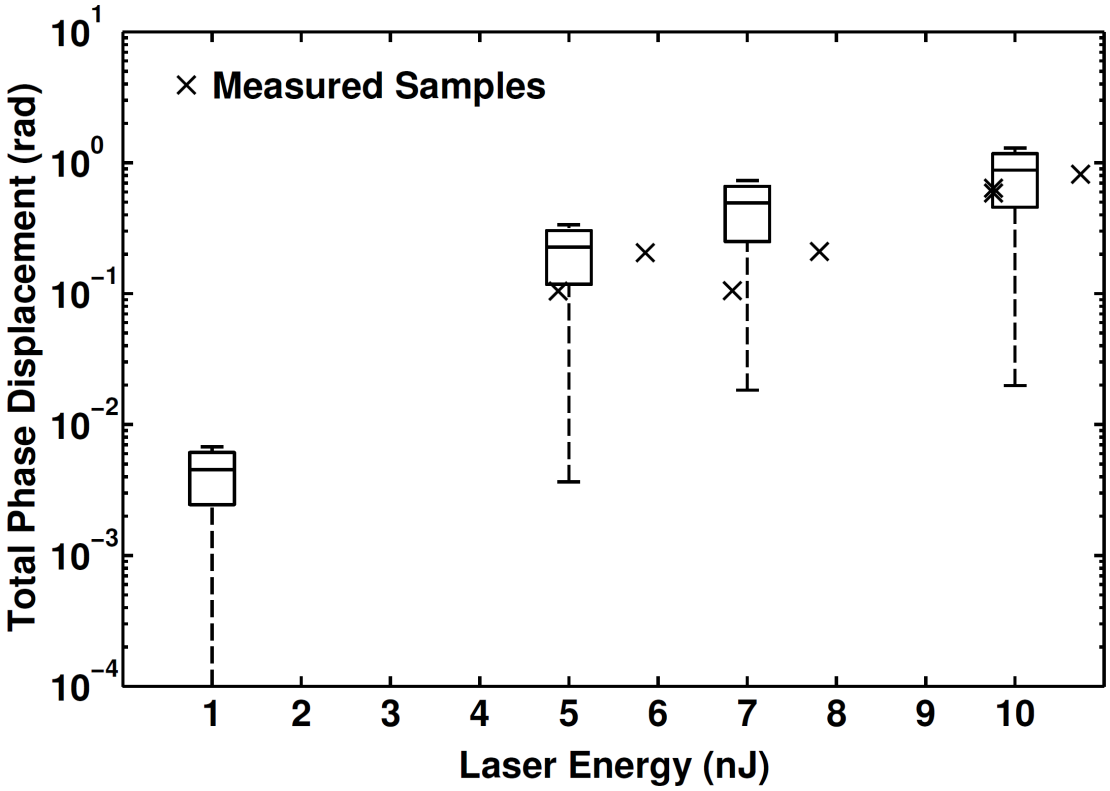


Figure 99: Total measured and calculated theoretical phase displacement across laser energy. The range of predicted values are given as box plots, where the box denotes median, first quartile, and third quartile. The whiskers denote data extents. Individual marks note measured samples.

analysis, the data from the 10 nJ exposures was collapsed, calculating the measured phase displacement and total transient duration. To compare these measured values to the expected values from the theory that has been developed, the induced charge metric at 10 nJ measured from Figure 96 was applied to the equations developed in [37]. From this framework, numerical calculations were performed in MATLAB to calculate the probability density of the phase deviation and transient duration as a function of laser energy. Figure 99 and Figure 100 overlay the results of these calculations with the experimentally extracted values. It can be seen that there is a general agreement between theory and experiment.

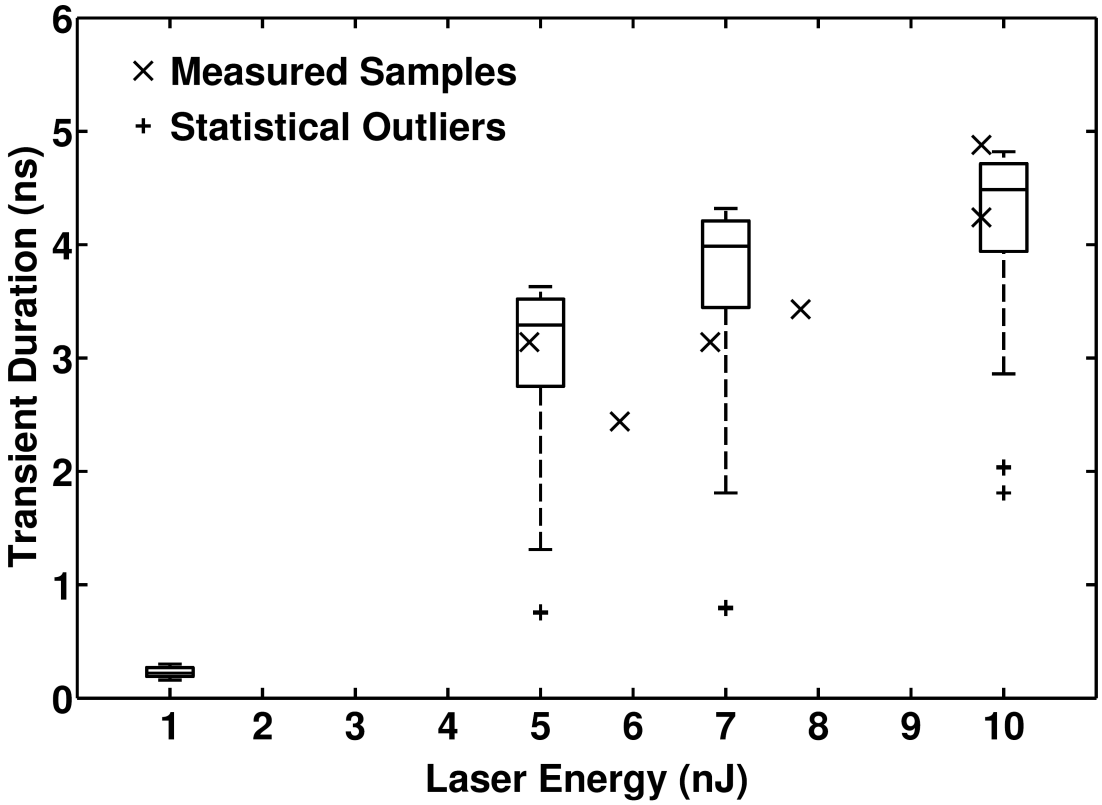


Figure 100: Measured and calculated theoretical transient duration across laser energy. The range of predicted values are given as box plots, where the box denotes median, first quartile, and third quartile. The whiskers denote data extents. Individual marks note measured samples.

7.1.3 Design Implications

By developing an analytical understanding of the origination of transient perturbations in resonant tank oscillators, we are able to make a number of design recommendations to enhance SET robustness. As we have demonstrated, the driving mechanism for transient perturbation of a resonant tank oscillator system is the voltage dispersion across the capacitor of the LC circuit, shown in (10). For a fixed quantity of injected charge, the voltage dispersion can be minimized by appropriate selection of the value of the capacitance. The resonant frequency of a tank oscillator is an under-determined system that is composed of both the inductance, L, and the capacitance, C; therefore, there are numerous solutions which provide an identical frequency tone. If we maximize the capacitance of the tank system, the dispersion of the capacitance voltage will be minimized. To verify this claim, two separate simulations of a resonant tank oscillator of identical resonant tone but varied capacitance value, were run for a similar induced charge. The results of this simulation are shown in Figure 101, which clearly illustrates the reduction in transient duration across all possible strike instances of the phase cycle for the oscillator with a larger capacitance. This reduction in capacitor voltage dispersion will also assist in preventing the occurrence of the third class of transient events, described as "collapse" transients, which occurs when large voltages across the capacitor (V_{CE} of the SiGe HBT) push the transistor into breakdown. This is a worst-case transient event which should be avoided at all costs.

This theory also allows us to make predictions for the impact of frequency scaling on the transient-induced oscillation perturbations. As the resonant frequency of the oscillator increases, the LC combination that composes the tank must be reduced in magnitude. Right away we can see that this scaling will put pressure on the maximum values of capacitance that will be feasible for a high-frequency oscillator design. This will inevitably lead to a larger voltage dispersion of the capacitance voltage for a fixed quantity of induced charge. Thus, it is expected that the impact of

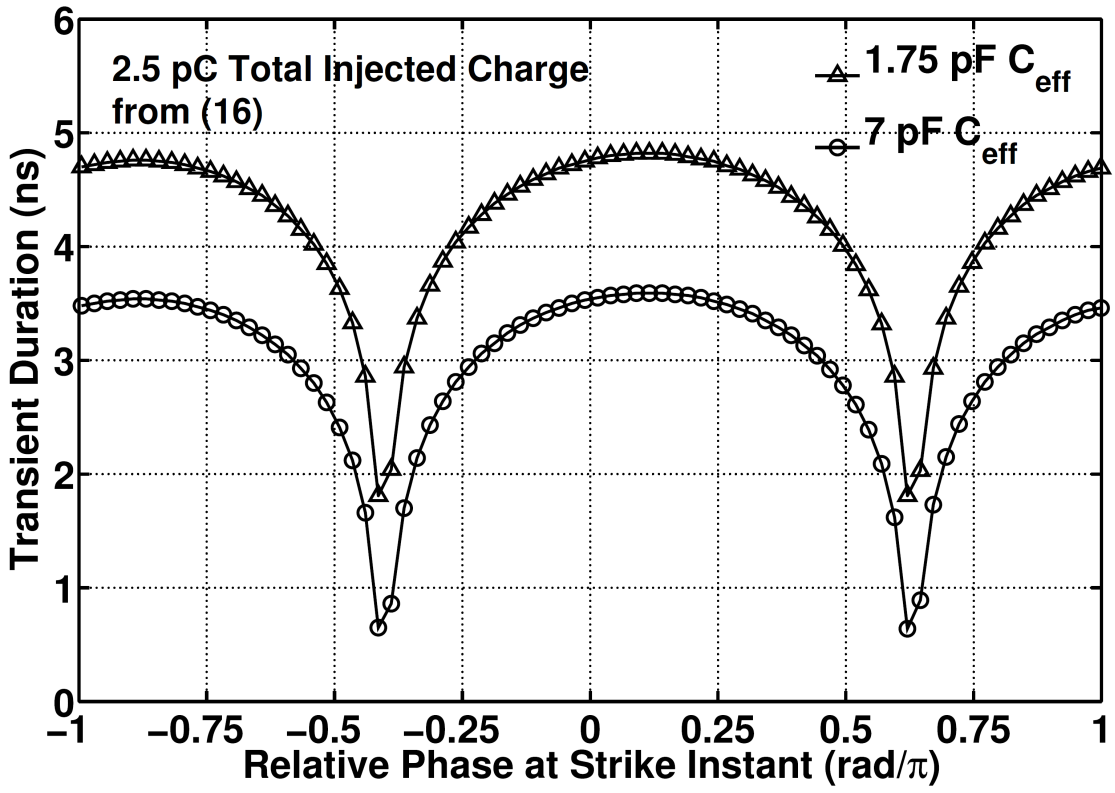


Figure 101: Simulated transient duration as a function of oscillator phase at strike instant, for multiple effective capactiance values.

transient perturbations will worsen with frequency scaling, for all types of characteristic transients. Furthermore, it can be expected that the frequency of "collapse" type transient events will increase as the resonance tone is scaled.

It has been demonstrated that transient perturbations in a resonant tank oscillator system are driven by the total charge that is induced by the SiGe HBT. Given that this is a charge-sensitive application, there are several technology recommendations which can be made to improve oscillator robustness to radiation-induced SETs. The first is the use of an SOI-based npn SiGe BiCMOS platform as opposed to a bulk npn platform. The presence of the buried oxide in an SOI system removes the subcollector-substrate junction from transistor cross-section. This junction has been shown in previous chapters to be efficient at collecting a large fraction of deposited charge in a semiconductor system. By eliminating this sensitive junction, a considerable portion of induced charge can be mitigated; however, this solution comes at the high cost of commercial SOI foundries. An alternative solution, which has been developed in Chapter 6, is to use inverse-mode biased devices for the cross-coupled differential pair. This technique has been demonstrated to reduce measured induced charges by 50

7.2 Single Event Effects in Charge Pumps

The charge pump block is an integral piece of the modern frequency synthesizer design, and has all but replaced the classical voltage-based phase detector circuit. The integrated phase-frequency detector charge pump block (common misnomer refers to both pieces as simply the phase-frequency detector) offers better locking capability, allowing phase lock to be obtained at any given offset frequency (given sufficient time). Previous voltage phase detectors were limited to offset frequencies closely matched to the desired lock frequency. To compensate for this limitation, op-amps were often employed as part of the voltage phase detector. This component however degraded the performance of the PLL by introducing additional noise and added both cost and

size to a design. The charge pump circuit precludes the need for op-amps as part of the phase-frequency detector, eliminating the losses imposed by this additional component [7].

The unhardened charge pump circuit has been identified as the Achilles heel of the PLL system from an SEE standpoint. The early work of SET investigations in digital PLLs immediately found the charge pump to be the most sensitive element of the closed-loop [15, 9]. Any charge which is induced on the charge pump is directly dropped across the loop filter, and directly affects the control bias for VCO. Unlike other transient perturbations which must traverse the loop and potentially experience feedback divisors which reduce phase offsets, all transient events originating from the charge pump will directly influence the output of the PLL. Since the recognition of the sensitivity of this block numerous methodologies have been employed, with varying degrees of success, to harden the charge pump circuit to SET events. All of these analyses have been performed for charge pump systems fabricated with MOSFET devices. In addition to sensitivity to SEEs, these systems are well-known to be highly susceptible to TID, which can significantly degrade the lifetime reliability of the PLL system.

The research performed in this document investigated an alternative charge pump topology, constructed from a complementary SiGe BiCMOS platform, which eliminates the TID sensitive MOSFET structures from the charge pump design. This circuit architecture is compared to both two other charge pump architectures constructed with MOSFETs from the same SiGe BiCMOS platform. The first architecture is a standard charge pump topology constructed with standard MOSFET devices. The second architecture uses the same architecture, but is constructed with enclosed gate devices. The TID comparison of these three architectures has been analyzed and reported in [36]. Presented in the current document is a comparison of the SEE susceptibility of the three architectures.

7.2.1 Charge Pump Architectures

The traditional CMOS-based charge pump architecture is shown in Figure 102. The basic structure is a combination of two opposite polarity current sources that are connected to the output node through a set of switches. The gate voltages of the switches are controlled by the phase-frequency detector. If the reference signal leads the VCO waveform in phase, the INC line goes high, sourcing current onto the loop filter capacitor. This raises the voltage of the output node and in turn increases the frequency of the VCO, bringing it in phase with the reference. Similarly, for a VCO signal that leads the reference in phase, the DEC line goes high, sinking current by pulling charge off the loop filter capacitor. This action induces the opposite effect, dropping the frequency of the VCO. This topology also incorporates a separate path for current when a switch is not engaged, maintaining the voltage headroom across the current sources for fast switching operation. An op-amp is also included, to mirror the voltage of the output node to the dummy node. By holding the dummy node voltage fixed, charge-sharing effects brought on by voltage differentials across parasitic capacitances are reduced, resulting in a reduction of switching spurs at the output.

The schematic in Figure 102 also illustrates the pieces of the charge pump cell that are sensitive to TID-induced damage. One will notice that the TID sensitive cells are isolated to the NMOS devices in the architecture, as these are the transistor that experience excess off-state leakage currents. PMOS devices only experience shifts in their threshold voltages, which are negligible for highly scaled technologies. There are two distinct TID-induced effects which can disrupt the operation of a charge pump operating in a radiation environment. These include increases in the off-state leakage of the nMOS active switch elements and the nMOS current source. Radiation-induced leakage will reduce the isolation of the switches, allowing charge to constantly flow into or out of the loop filter. This constant flow of charge will result in constant adjustment by the charge pump to maintain a locked state. Similarly, changes in

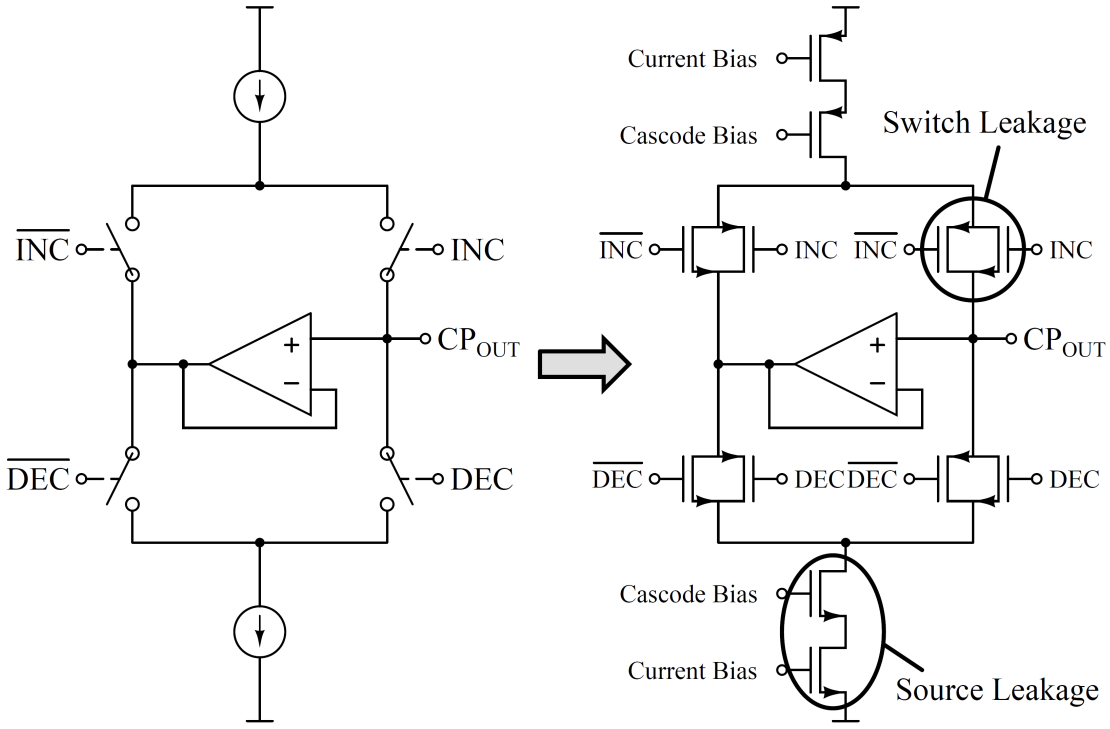


Figure 102: A schematic representation of a typical CMOS charge pump circuit for PLL applications. The TID sensitive regions are highlighted.

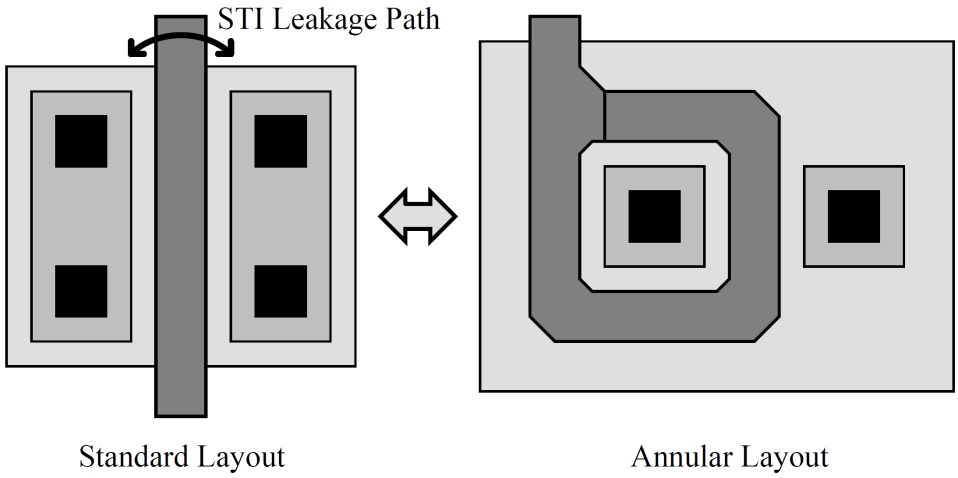


Figure 103: Top-down comparisons of a standard single-finger MOSFET and an identical enclosed-gate MOSFET.

the leakage current of the current source could give rise to a mismatch between the sinking and sourcing currents of the charge pump. Both of these effects produce spurs in the closed-loop phase noise response of the PLL [7]. The introduction of these spurs has been shown to directly contribute to the front-end bit error rate in a frequency synthesis application [67].

To combat this TID sensitivity of the standard CMOS charge pump cell, two alternative architectures have been proposed. The first of these architectures uses the same topology as Figure 102, but replaces the standard MOSFET cell with an enclosed-gate layout (EGL) cell [12]. The translation of a standard MOSFET cell to an EGL architecture is shown in Figure 103. By completely enclosing the source/drain of the MOSFET device with the polysilicon gate, any shallow trench isolation overlap between source and drain is eliminated, removing the parasitic channel that forms from trapped charges and interface traps in the oxide. The EGL device is less compact than traditional layouts, consuming more die area. Given that this a custom device structure, no current industry supported models are available as part of a design package. Although the W/L ratio of the EGL device can be roughly estimated to

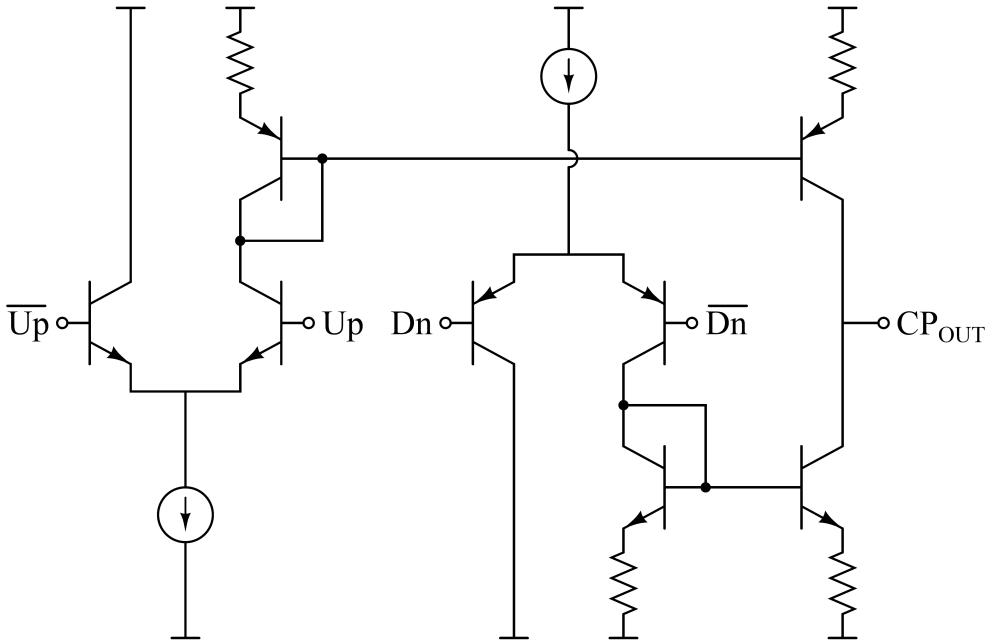


Figure 104: Schematic of a charge pump built upon complementary SiGe HBTs.

match a standard stripe CMOS cell, the parasitic capacitances will be significantly different between the two structures.

The second architecture that has been proposed to combat the TID sensitivity of the standard CMOS charge pump cell is a bipolar-only charge pump architecture. The schematic for this architecture is shown in Figure 104. The design is only possible with the incorporation of performance-matched *pnp* HBTs, which are provided in Texas Instruments CBC8 complementary SOI SiGe BiCMOS platform. Noticeable changes in circuit topology are apparent for the SiGe HBT design. These changes are necessary to preclude the HBT from entering the saturation region of operation. By using a current steering scheme similar to high-speed current-mode logic cells, the differential switches can provide the same source/sink current capability as the standard charge pump cell. This drawbacks to this design include a reduction in output resistance (a direct result of the inability to employ a cascoded topology given the larger headroom required by the HBT), and increased power dissipation.

7.2.2 Heavy-Ion Broadbeam Measurements

These designs have been directly compared, post TID-radiation, demonstrating the enhanced immunity of the SiGe HBT charge pump to TID-induced current degradation. The EGL design was found to have an unexpected sensitivity which was discovered to be related to a layout-induced mechanism which can be easily eliminated. It is of equal interest to the space radiation effects community to understand the impact of the SEE-induced events on the different design topologies. To explore this angle, the three designs were packaged and measured in a heavy-ion broadbeam environment. The packages were custom-designed PCBs with control lines for the switches, incorporating CPW transmission lines built on a Rogers 4003c dielectric. The structures were irradiated at LBNLs 88-inch cyclotron facility, using the 10 MeV/u ion cocktail.

To conduct these measurements, the charge pumps were biased in the tri-state mode of operation while in the ion beam. The transients generated were measured as a voltage across a known load resistor connected in series with a power supply. This mimicked the voltage maintained by the loop filter in a closed-loop configuration of a PLL system. The voltage conditions on the output of the charge pump were tested at mid-rail and at 0.5 V from the rail to observe variations in error cross-section. Transients were detected by using a fast-frame window trigger on the oscilloscope that detected deviations outside the nominal steady-state conditions. A typical transient waveform generated by a charge pump strike is shown in Figure 105. Three important metrics that will be used to describe these transients are the peak current, duration, and total collected charge. Peak current is the maximum current deviation induced by the ion strike. The transient duration is defined as the full width of the initial transient pulse at half its maximum value (FWHM). The total collected charge is calculated by integrating the transient current waveform. With these three metrics, the data sets obtained for all three charge pump architectures were collapsed and plotted.

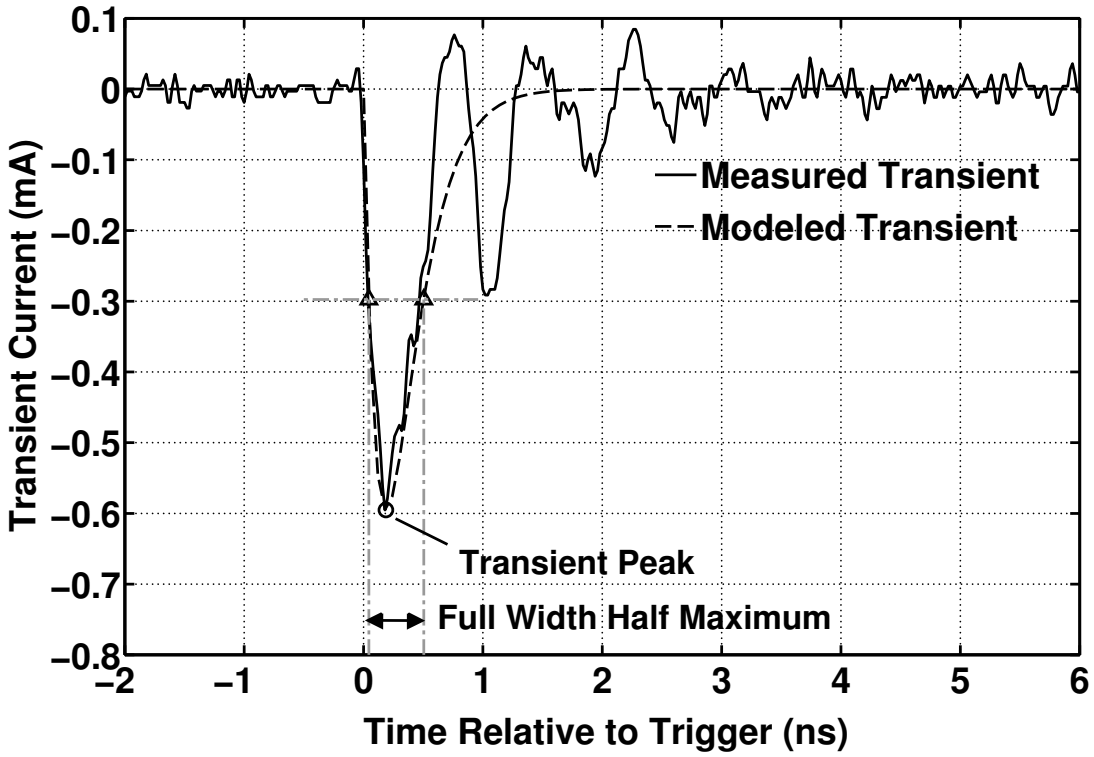


Figure 105: Time-domain waveform of a typical charge pump SET.

7.2.3 Single Event Effect Implication and System Impact

A visualization of each measured transient for all three charge pump architectures is shown in Figure 106. This plot is similar to those developed in [11], and shows each transient as a function of the two extracted metrics we have defined previously that compose the total collected charge. The dotted lines in the figure show the approximate total induced charge as a function of the peak current and FWHM, assuming a double exponential fit to the transient current. The dashed lines show the minimum resolution set by the measurement set-up and equipment. The MOSFET designs show tight groupings with larger peak current, generally corresponding to strikes of greater LET. Transient duration in the MOSFET designs is also a relatively consistent value. Meanwhile, the HBT transients are spread out over the range of possible transients, with no coherent grouping. A breakdown of the HBT transients shows that while small LETs consistently produce small charge collection, large LETs

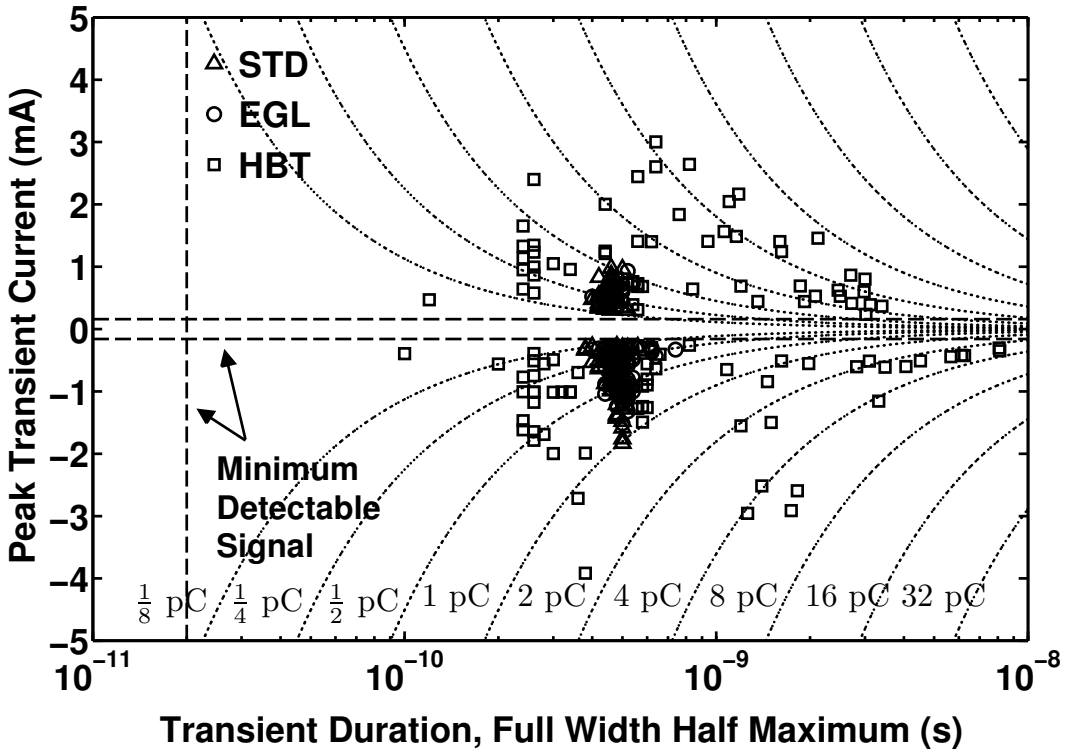


Figure 106: Distribution of transients for the three charge pump architectures based on their peak current and FWHM duration.

are equally likely to produce large or small charges. This visualization provides the most effective means to determine which transients will produce errors in the closed-loop output of the PLL system.

From the derivation of closed-loop transient response in [55], it becomes apparent that the total excess charge put onto the loop filter will be the appropriate magnitude metric for the charge pump. That paper derives the recovery time from a charge pump transient as

$$t_{rec} = \frac{Q_{SET}}{I_{CP}} + t_{SET} \tag{13}$$

where I_{CP} is the nominal output current of the charge pump and t_{SET} is the transient duration. A critical threshold for maximum closed-loop transients is also derived that is dependent on the closed-loop dynamics of the system. According to this derivation,

the threshold time for maximal phase disruption of the PLL is given as

$$\tau_{crit} = \frac{f_{LO}}{N\omega_n^2} \tag{14}$$

where f_{LO} is the nominal output frequency of the synthesizer, N is the VCO frequency divisor for comparison with the reference phase, and ω_n is the natural frequency of the feedback loop, in radians. For lack of better measurement evidence, it has been assumed that τ_{crit} is the minimum condition to produce an error in a wireless bit stream communications link. The minimum transient charge to produce this condition is thus

$$Q_{SET} > \frac{I_{CP} f_{LO}}{N\omega_n^2} - I_{CP} t_{SET}. \tag{15}$$

Any transient producing charge greater than this condition will be considered an error, while any transient producing less charge can be discarded as not producing an actual bit error. An effective error cross-section for the analog charge pump can therefore be accurately stated. This analysis is likely over-simplified, as a single transient strike on the charge pump can cause more than a single bit error in the wireless data stream, but as mentioned previously, a complete theory for translating synthesizer transients to receiver bit errors does not presently exist.

As an example of what this analysis means physically, consider a worst case scenario. Assume the comparison frequency at the phase frequency detector, f_{comp} , is ten times greater than the natural frequency, in Hertz. This is the minimum ratio required to make linear approximations for the mixed signal PLL. Also note that by definition, $N = f_{LO}/f_{comp}$. The term $I_{CP} t_{SET}$ can be assumed to be negligible based on the data in Figure 106. Therefore, under these conditions, the critical charge to produce errors reduces to

$$Q_{SET} > \frac{100 I_{CP}}{4\pi^2 f_{comp}}. \tag{16}$$

Since each of the charge pumps investigated were designed for a nominal output of 1 mA, even a comparison frequency of 100 MHz would require a charge of approximately 25 pC

to produce an error at the output. As shown in Figure 106, even the largest transients produced by the HBT charge pump are around 7 pC. Under these assumptions therefore, despite the large and erratic transients produced by the HBT design relative to the MOSFET designs, both should be single event immune as built. It is assumed that SiGe SOI process technology has played a role in minimizing this collected charge to achieve this result.

However, since the true impact of SEE on bit errors is unknown, consider a scenario where the critical charge for an error were an order of magnitude less, or 2.5 pC, which might be achieved if the charge pump current were dropped to 100 μA. The error cross-section curve for this assumption is shown in Figure 107. The first plot shows a baseline cross-section of all transients captured. Figure 108 discards all transients with a total collected charge below 2.5 pC. Even under these assumptions, all of the transients captured in the MOSFET charge pumps in Figure xx would be negligible. However, a subset of the HBT charge pump transients are large enough to generate errors. Thus, despite its significantly smaller die area, the HBT shows a higher cross-section than both MOSFET designs. However, the saturated cross-section values are low thanks to the thick-film SOI layer and would not contribute significant errors to the system.

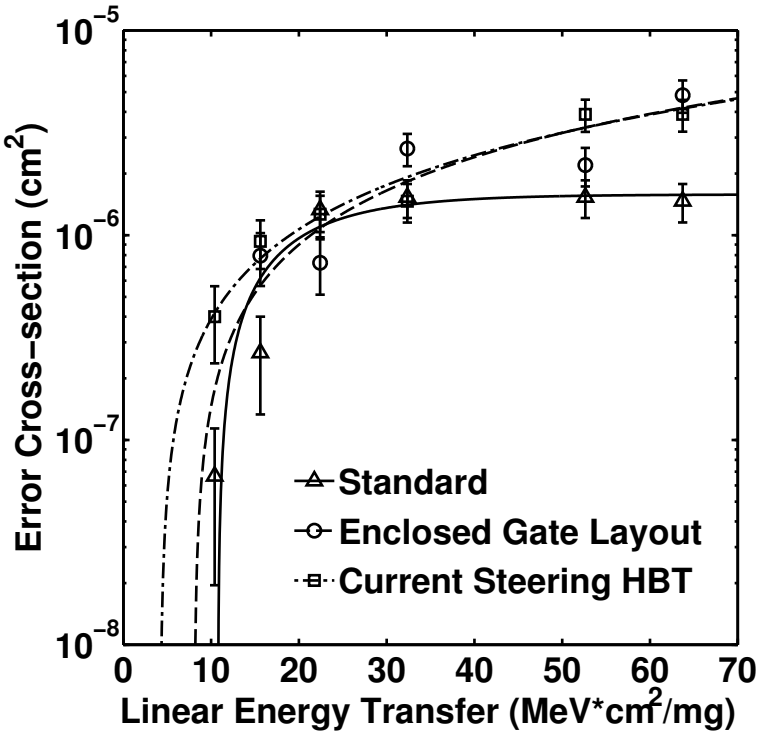


Figure 107: Error cross-section of the three charge pump designs under the condition of all error events being considered.

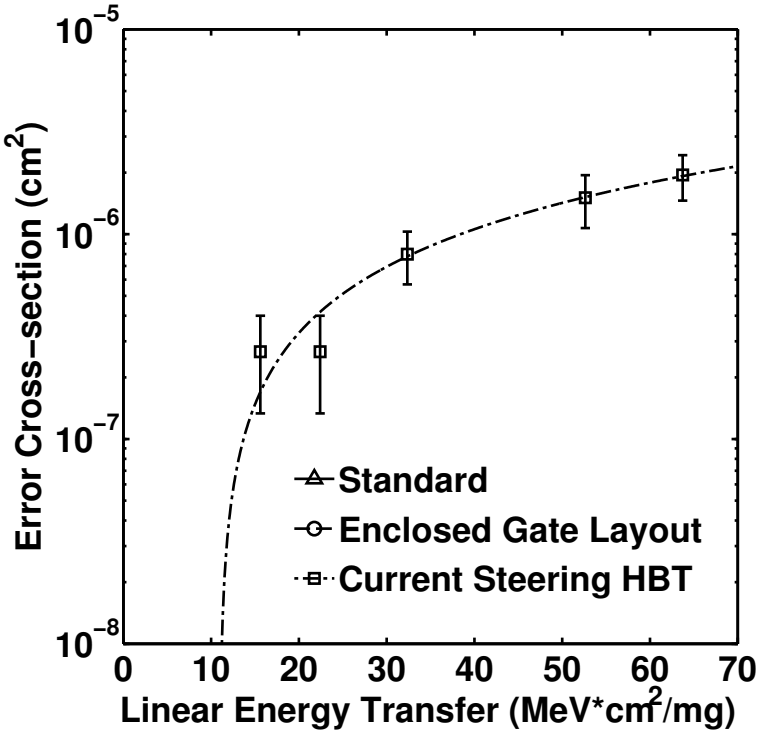


Figure 108: Error cross-section of the three charge pump designs under the condition of only events generating more than 2.5 pC of charge being considered.

7.3 Single Event Effects in Frequency Dividers

Frequency dividers are an integral piece of a frequency synthesizer system. As demonstrated from (7), frequency dividers in the feedback loop of a PLL system serve to scale the frequency of the VCO to a desired resonant tone. From Figure 93, it can be seen that two classes of dividers are commonly found in a frequency synthesizer PLL. These dividers include the R-Divider and the N-Divider. Both are programmable dividers, to extend the functionality of the system; however, their architectures can vary significantly. The R-Divider is most commonly implemented as a chain of divide-by-2 cells with control lines to allow selective division ratios to be extracted from the chain. This structure can be implemented in either CMOS or bipolar technologies, depending on the input frequency of the reference signal. The N-Divider can be a much more complicated structure, depending on the frequency range of the VCO. For frequencies in the GHz range, traditional digital CMOS counters are unable to respond adequately to provide the division. To compensate for this speed difference, prescaler blocks fabricated from higher-speed bipolar cells are often employed to scale down the frequency to a range that is compatible with digital CMOS counters. This allows most of the N-Divider structure to be implemented with primarily low-power, highly-integratable digital cells.

Previous studies of digital dividers for DPLL applications have been performed for highly-scaled CMOS technology platforms [56, 55, 9].l The work of [31] has demonstrated that the location and gain of the frequency dividers in a PLL configuration can have a strong influence on the predicted error rate. The authors of [56] collapsed their data using a figure of merit they defined as the phase displacement induced by particle upsets. The phase displacement can be defined as

$$\phi_{disp} = \frac{2\pi|T_e - T_{clk}|}{T_{clk}} = |T_e - T_{clk}|\omega_{clk} \tag{17}$$

where T_e is the erroneous clock period, T_{clk} is the normal period of oscillation, and

ω_{clk} is the PLL radial frequency. With this metric, the authors were able to form a probabilistic study of divider errors on the response of the PLL, built on a general framework of the loop characteristics of the system. Only one previous study of divider architectures built from SiGe HBTs has been performed in the past, where the frequency of error occurrence was found to be independent of the division state of the divider [88]. In the current work, the SEE impact of an alternative R-divider architecture is investigated, built from 1st generation, SOI SiGe HBTs. Additionally, three alternative quad-modulus prescaler architectures are investigated for SEE sensitivity for an N-Divider. Finally, the impact of the digital counter of the N-divder is explored in the context of the full PLL system.

7.3.1 R-Divider Broadbeam Analysis

Two separate architectures of R-divider cells were tested in the current study; these included R-divider blocks assembled from standard current-mode logic (CML) flip-flop cells and gated-feedback cell (GFC) CML flip-flop cells. The GFC architecture has been published as a successful technique for improving the SEU sensitivity of CML master-slave flip-flop cells assembled with SiGe HBTs. Both R-divider structures included four daisy-chained divide-by-2 blocks to form a conglomerate divide-by-16 divider cell. Both R-divider architectures were fabricated using the previously described Texas Instrument's CBC8 SiGe BiCMOS technology process, and individually packaged on high-speed custom-design PCB boards. A differential input clock frequency of 1 GHz was used as the reference signal, which provided a divided differential output clock frequnecy of 62.5 MHz. Both R-divider variants were brough to the Texas A&M Cyclotron Institute and tested with multiple 15 MeV/u ion beams to provide a spectrum of ion LETs to generate an event cross-section for both structures. The divided clock output of the R-divider block was fed into a high-speed, real-time sampling oscilloscope such that the time-domain information was saved for every

trigger/error event. An error event for the R-divider was defined to be a modulation of the nominal pulse width of the output signal.

There were two characteristic error signatures measured for both R-divider architectures, including erroneouse pulses randomly distrbuted throughout the output period of the clock and elongated pulses of the normal clock period. Figure 109 shows an erroneous pulse where the ion-strike produces a brief change in state not associated with a clock edge before returning to the nominal state. This transient signature produces the largest errors because the edge-detection circuitry of the PFD will interpret this change as a significant variation in the output frequency of the divider as defined in (17). An erroneous pulse occurs if one of the two flip-flop cells within a divide-by-2 architecture experiences a bit upset directly following a clock transition that latches the data input within the flip-flop cell that experiences the upset. Figure 110 shows a second transient classification where the existing period of oscillation is merely elongated from its original for one period, producing much smaller variations in frequency. This brand of transient occurs if the SEU event in a flip-flop originates prior to the clock transition resulting in a latch of data for that cell. The impact of these variations on the output of the frequency synthesizer will depend in large part on the dynamics of the closed-loop system. A narrow loop bandwidth PLL might not show any influence from the strike because the long time constant around the loop reducesthe influence of a single-cycle deviation, while a wide loop bandwidth may disturb the phase of the steady-state output waveform.

Calculating the total pulse width dispersions for an accumulated fluence, a cross section-curve can be generated for both the standard and GFC R-divider. These error cross-section curves, plotted in Figure 111, are a measure of the frequency of occurence of the defined error condition; however, no information of the ϕ_{dsip} can be extracted from the curve for either R-divider variant. It is found that the GFC architecture has an elevated error cross-section as compared to the standard architecutre, a result

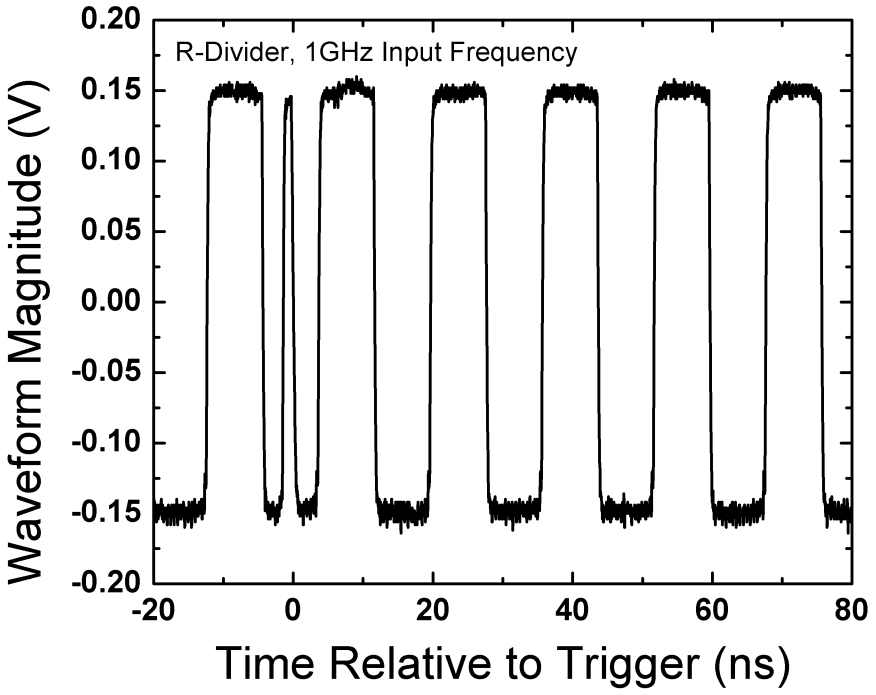


Figure 109: Measured characteristic erroneous pulse transient of an R-divider exposed to heavy-ions.

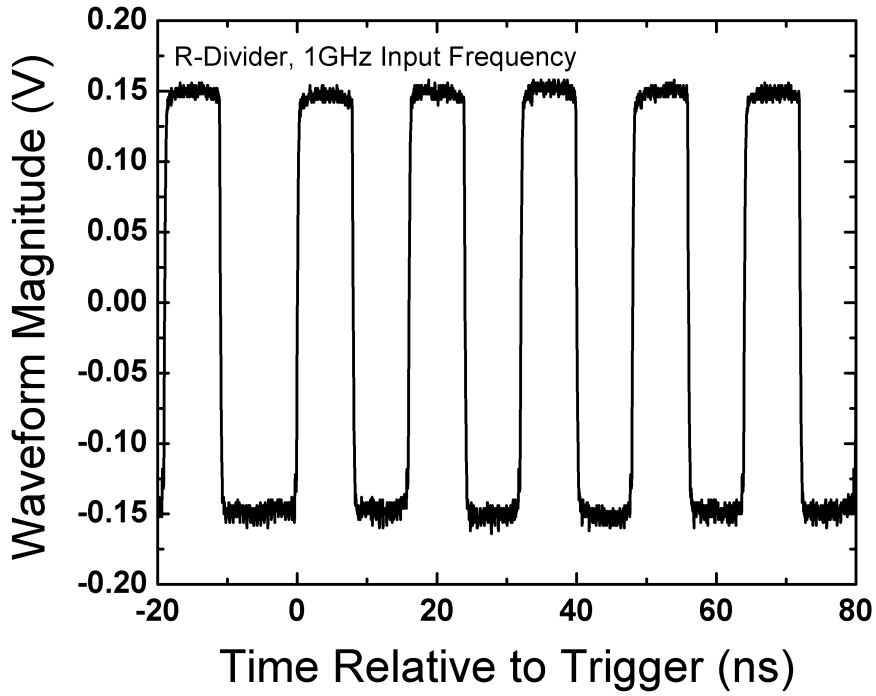


Figure 110: Measured characteristic elongated pulse transient of an R-divider exposed to heavy-ions.

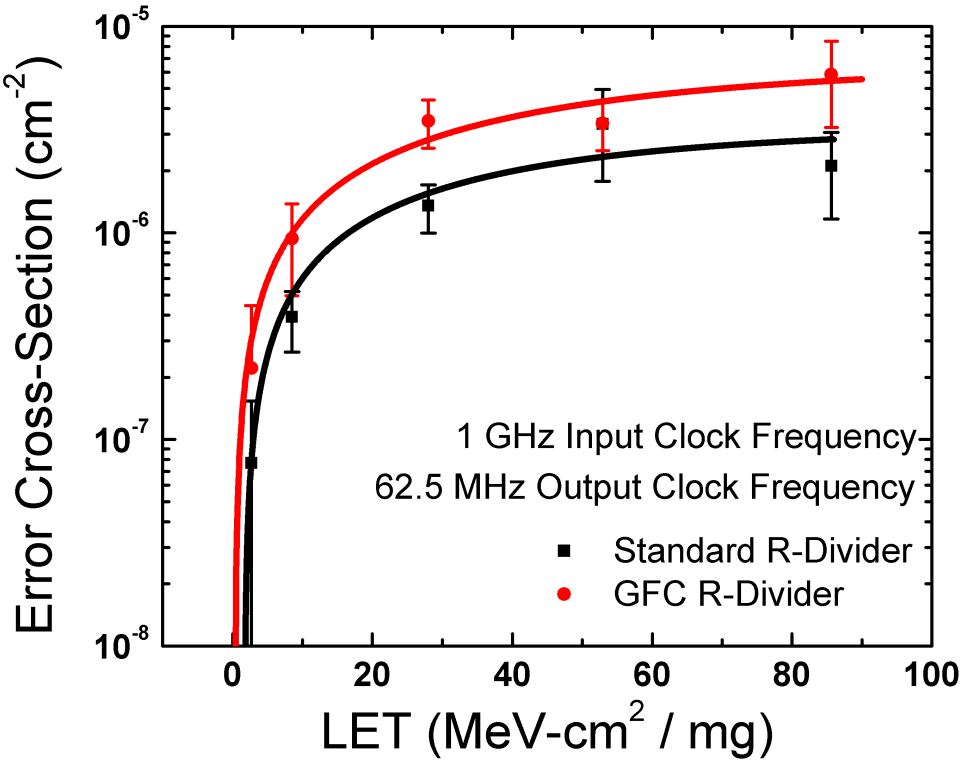


Figure 111: Comparison of error cross-section for R-dividers built from GFC and standard CML latch architectures.

which is contradictory to the previous measurements of GFC digital shift registers. To investigate this discrepancy, GFC 16-bit digital shift registers were constructed in the same technolgy (CBC8 process) and compared to a standard architecture 16-bit digitl shift register. Heavy-ion broadbeam measurements on these two structures revealed the same trend as seen by the R-divider structures, with an elevated error-cross section for the GFC architecture. Looking back at the original data set, it was found that the device-to-device spacing of the HBTs within the design was an order of magnitude larger for the GFC architecture (giving a total register size of 3 mm x 1 mm), as compared to the standard architecture (only 1 mm x 1 mm). Both the GFC and standard R-dividers and shift registers for the current study had identical HBT spacing, leading us to believe that improvement in error cross-section for the previous work was linked to the HBT-to-HBT spacing as opposed to the internal redundancy added to the latch.

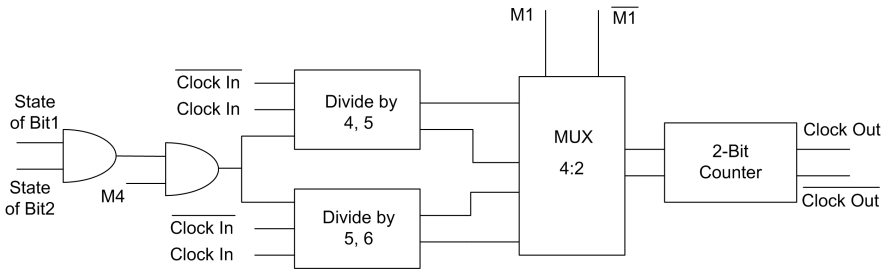


Figure 112: A block diagram of a custom-designed asynchronous quad modulus prescaler.

7.3.2 N-Divider Architectures

The N-divider component is a second frequency divider block that seves a vital role in the Integer-N frequency synthesizer system. This component is composed of both a frequency prescaler coupled together with digital counters to provide a lumped, programmable dividor to the loop feedback for frequency synthesis. The prescaler structures must be able to divide down high frequency (¿ 1 GHz) input clock signals, and as such are often constructed with SiGe or III-V HBT technologies. The most common prescaler implementations are single modulus, dual modulusm and quad modulus prescalers. The most basic prescaler architecture, the single modulus prescaler, sacrifices phase noise for closer spaced channels by only allowing N-values that are integer multiples of the prescaler divisor. Dual modulus and quad modulus architectures alleviate this issue by providing a pulse-swallow function. The quad modulus prescaler, while the most complex, provides the lowest minimum continuous divide ratio of all the prescaler architectures. This circuit is realized with a single prescaler, a pulse swallow circuit, and a four-pulse swallow circuit. In the current study, the SEE sensitivity of an N-divider block built with a quad modulus prescaler was investigated for SEE sensitivity.

Three prescaler architectures were fabricated to investigate the architectural impact of the prescaler on the heavy-ion induced SEE rate. The first quad modulus prescaler developed incorporated two standalone dual modulus prescalers that were mutliplexed

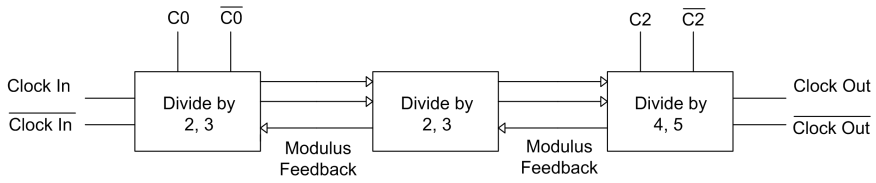


Figure 113: A block diagram of a cascded 16/17/20/21 synchronous quad modulus prescaler.

to feed a 2-bit counter. A diagram for this circuit is shown in Figure 112. Two sets of control lines, one for the pulse-swallow functionality of the two dual modlulus prescalers and one for directing the selection of the frequency division for the multiplexer, are included to provide the capability of division ratios of 16, 17, 20, and 21. This architecture is limited in its application for the full N-divider as the current version is asynchronous and N-divider operation requires a synchronous prescaler. The circuit is still useful from an SEE comparison standpoint for other synchronous prescaler architectures. The second quad modulus prescaler architecture was identical to the asynchronous variant; however, the CML flip-flop cells of the dual modulus prescaler blocks were designed using the GFC topology. The final quad modulus architecture includes a number of divide by 2/3 dual-modulus cells cascaded with a divide by 4/5 dual-modulus cell in a ripple fashion as shown in Figure 113. This architecture includes two control lines that similarly provide the capability to form a divide-by 16/17/20/21 cell. Of the three prescaler architectures, the synchronous ripple divider employed the smalled number of HBT cells.

The full N-divider architecture is formed by integrating the quad modulus prescaler with three digital CMOS counters (referred to as the A, B and C counter). Both the A and B counters are programmable two-bit counters, while the C counter is a programmable eight-bit counter. All three counters are clocked in parallel from the output of the quad modulus prescaler block. Initally the prescaler divides the input clock frequency by 21, clocking all three digital counters at this rate, until either the B or the A counter reaches a value of zero. At this point, the prescaler either divides by

17 or 20, depending on which of the two counters has reached counted down completely first. Once both the A and B counters have reached zero, the prescaler divides by 16 until the C counter has reached zero. At this point, all three digital counters are reloaded with their programmed inital values, and the countdown sequence repeats. This behavior results in a programmable division ratio that can be determined from the initial values of the digital counters using (18).

$$N = (16 \times C) + (4 \times B) + A \tag{18}$$

7.3.3 Heavy-Ion Broadbeam Analysis

Prior to testing the full N-divider cell in a broadbeam environment, the standalone prescaler circuits were tested to quantify their contributions to the full error cross-section of the N-divider and compare the various architectures that were fabricated. The three variants were each packaged on custom-design high-speed PCBs to preserve the clock integrity coming on and off the PCB. Each prescaler was fixed for a static division state for each programmable divisor (16/17/20/21) and fed with an input clock frequency of 1 GHz. The packages were irradiated at LBNL's 88-inch cyclotron facility using the 10 MeV/u ion cocktaiil. Multiple normal-incidenct ion species were employed to provide a spectrum of ion LET values. Similar to the R-divider measurement, the output of the prescaler circuits was fed into a high-speed oscilloscope, such that any deviations in the output clock frequency could be directly captured. To assemble error cross-section curves for the prescaler variants, an error criteria similar to the R-divider (deviation in pulse width) was established. The measured error cross-section curves for the three prescaler architectures are plotted in Figures 114-116.

Although not represented in the error cross-section representation of the data, the transient signatures measured for each prescaler architecutre are identical to the R-divider transients. Namely, two characteristic transient waveforms were measured,

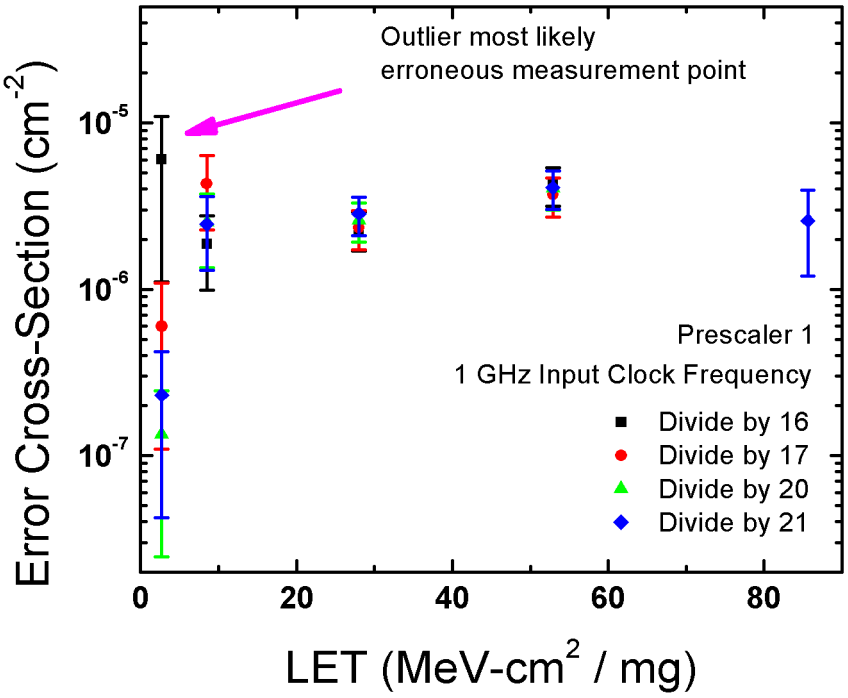


Figure 114: Measured error cross-section curves for an asynchronous quad modulus prescaler constructed with standard CML flip-flops operating statically in each division state.

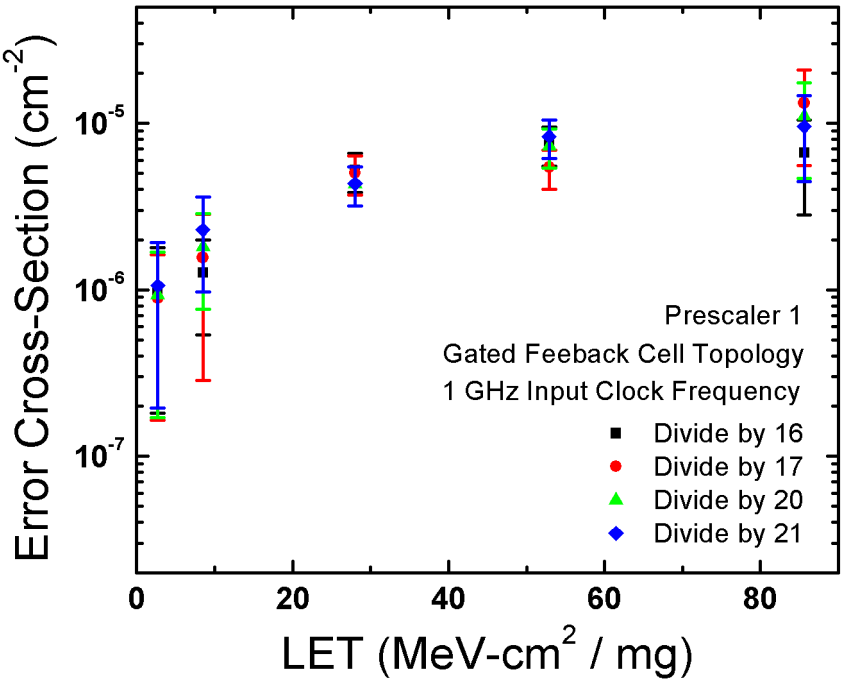


Figure 115: Measured error cross-section curves for an asynchronous quad modulus prescaler constructed with GFC CML flip-flops operating statically in each division state.

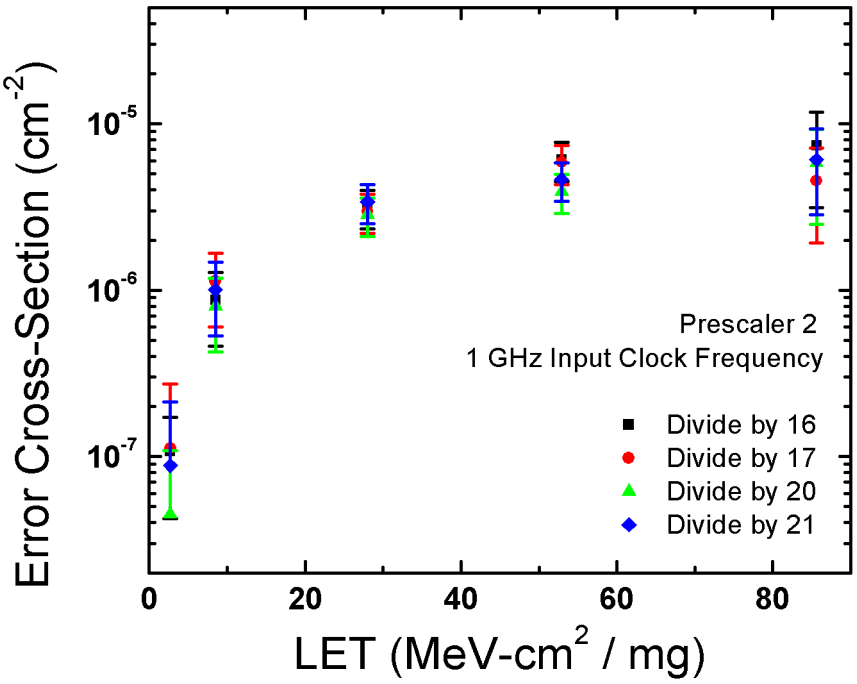


Figure 116: Measured error cross-section curves for a synchronous, ripple quad modulus prescaler constructed with standard CML flip-flops operating statically in each division state.

erroneous pulses and elongated pulses. Again the erroneous pulses serve as a worst-case condition for introducing phase error to the PFD cell of the full PLL system. From the error cross-section curves, several key pieces of information can be extracted. The first is that the frequency of error occurence is not dependent on the division state of the frequency divider. This result complements previous studies of SEE in SiGe frequency dividers. Although there is no dependence on the division state, a dependence on architecture is evident from the measured curves. The GFC variant of the asynchronous prescaler has the largest error cross-section, which agrees with the R-divider data gathered earlier. The increase in cross-section is attributed to the increase in the HBT count of the GFC register, despite the addition of local redundancy. Both asynchronous prescalers however are found to have a higher cross-section as compared to the synchronous ripple prescaler, especially for low ion LETs. This result is a direct consequence of the reduced HBT count of the synchronous, ripple prescaler.

From these measured results it is clear that the synchrnous prescaler is the optimal choice for integrating the full N-divider.

Building upon the learning gained from the prescaler studies, a full N-divider was designed and fabricated using the CBC8 technology process. This circuit block included a synchronous, ripple quad modulus prescaler, digital CMOS counters, and a memory map for storing the prgorammed division values. The programming of the memory map was accomplished with a three-wire serial peripheral interface (SPI). The three-wire communication was controlled with an off-chip FPGA that allowed the user to customize the division rate of the N-divider cell. The full circuit was packaged with a custom-designed PCB and brought to LBNL's 88-inch cyclotron for heavy-ion broadbeam testing. The input clock frequency was fixed at 1 GHz and the N-divider was programmed to divide the clock by 128 to give an output frequency of 7.812 MHz. The output of the N-divider was fed into a high-speed oscilloscope such that any deviations in the output clock frequency could be captured. Multiple ion species from the 10 MeV/u beam cocktail were employed to capture a spectrum of space-relevant LETs. For each experimental run to a fixed accumulated ion fluence, the number of erroneous frequency pulses were recorded such that event cross-section curves could be calculated.

The measured event cross-section of the full N-divider is overlayed with the cross-section of the stand-alone quad modulus prescaler in Figure 117. While similar in shape, the event cross-section for the full N-divider is larger than the stand-alone prescaler by nearly an order of magnitude for every measured ion LET. To understand this increase in error-cross section, the distribution of instantaneous erroneous frequency divisions, plotted in Figure 118, was assembled for all of the experimental runs. The nominal division frequency for the N-divider was the programmed value of 128; hence, a noticeable absence of "erroneous" frequencies can be seen at this value. Interestingly, this distribution plot demonstrates that erroneous division values are centered closesly

to the programmed value, differing only by an upper integer value of five. The measured error cross-section curve is dominated by these types of errors, while impose only a small phase error to the PFD and will likely not cause a loss of system lock. These small frequency errors are attributed to errors arising within the quad modulus prescaler, buffer cells linking the prescaler with the digital counters, and the A & B CMOS counters. Figure 118 also demonstrates several large, ion-induced frequency deviations in the output clock signal of the N-divider. These errors arise from upset bits within the C digital counter. Any SEU occuring within the C counter will result in a the output frequency being divided down by the integer value of the quad modulus prescaler divisor (in this case, 16) multiplied by the difference in the value of the upset counter with its pre-strike value. The acutal error in frequency division will be randomly distributed across all possible counter values as the frequency error depends on both strike location and strike time duringthe count-down sequence. These types of errors can easily result in a loss of lock for the closed-loop PLL as significant phase error is potentially introduced to the PFD.

A second class of errors that were measured, but not plotted here, are SEUs that occur within the memory map of the N-divider. These types of errors are an absolute worst case scenario for SEEs in frequency synthesis PLL systems, as the system can not be restored to its pre-strike operation until a user-initiated reprogramming of memory map is performed. This type of error is known in the literature as a Single Event Functional Interrupt (SEFI). As any SEFI within the N-divider results in a loss of operation until the system is cycled in power and reprogrammed, this sensitivty must be addressed with hardnening methodologies. The most effect means of hardening the memory map is to use physical redundancy of the memory registers coupled with a voting scheme, such as a triple-mode redundancy topology. As the memory map is composed of minimum-sized CMOS registers, triplicating the register bank results in a negligible increase in system area as compared to the full N-divider. A similar

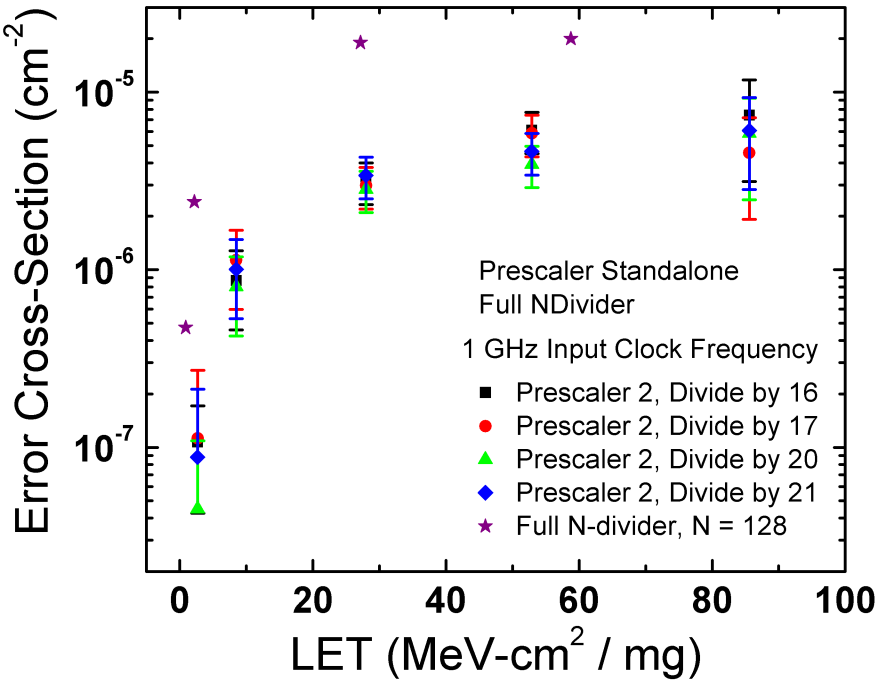


Figure 117: Measured error cross-section curves for a full N-divider programmed to operate in the divide-by-128 state.

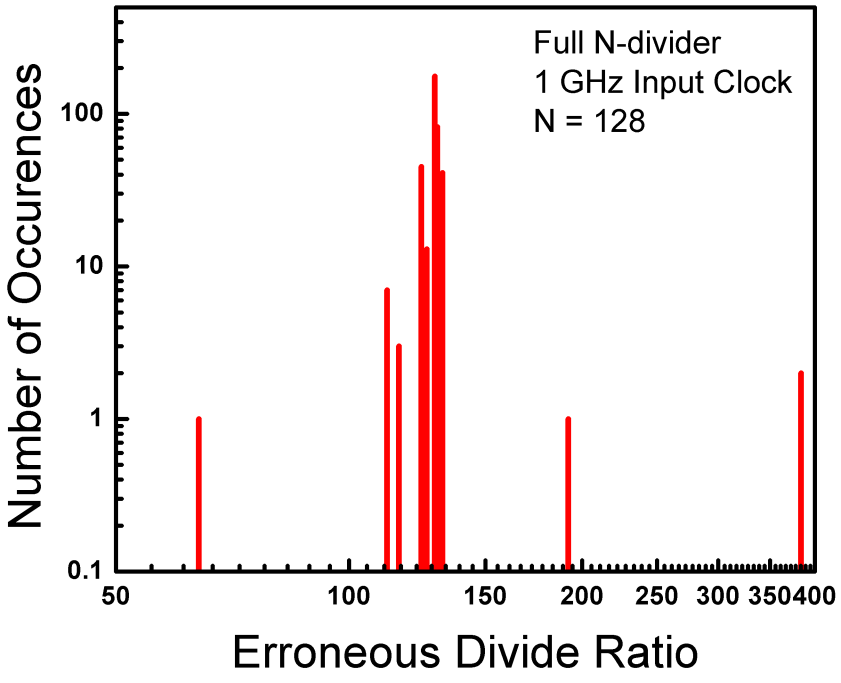


Figure 118: Distribution of measured instantaneous erroneous frequencies of the N-divider for all experimental runs, encompassing multiple ion species and associated LETs.

redundancy scheme can be employed on the A, B, and C counters that will assist in mitigating the occurence of the large erroneous division frequencies and improve the single event immunity of the frequency synthesizer PLL.

CHAPTER VIII

CONCLUSIONS

SiGe technology, while nearly immune to TID damage for nominal orbital mission durations, has repeatedly been found to be susceptible to SEE for standard circuit architectures. Addressing this sensitivity requires system designers to incorporate RHBD techniques, either device or circuit-level, into their circuit topologies. The most desirable RHBD strategies would be device-level modifications that allow designers to maintain existing circuit topologies while mitigating the effects of radiation-induced transient currents. This dissertation has focused on developing a comprehensive understanding of the origination of ion-induced transient currents in SiGe HBTs and applying this knowledge to the development of device-level hardening methodologies to improve the susceptibility of SiGe system to ion-induced sngle event effects. The work performed has relied heavily on 3D TCAD software packages to provide insight into the dynamics of ion-induced free carrier redistrubition within the HBT following a strike event that give rise to the induced transient currents. Heavy-ion irradiation from terrestial accelerator facillities and sub-bandgap pulsed-laser studies supplement the simulation data with experimental insights. Equipped with these tools, mutliple device-level radiation hardening methodologies have been explored for their efficacy of mitigating SEE-induced phenomena and possible application in SiGe systems. In addition, investigations into complex, mixed-signal SiGe circuits has been performed to gain an understanding of system-level SEE sensitivity and the appropriate hardnening techniques that can be applied.

Many contributions to the body of knowledge of radiation effects in SiGe HBT systems have arisen from the research performed in this disseration, as evidenced

by the numerous peer-reviewed publications. The predominant contributions of this dissertation are summarized here:

- The basic mechanisms giving rise to ion-induced transient currents in SiGe HBTs. These mechanisms haven been characterized using calibrated 3D TCAD simulations of multiple device topolgies and platforms. The fundamental limitation of the transient response was identified as the ion-induced shunt current that is formed between the collector and emitter terminals. The low threshold-LETs of digital shift registers constructed from SiGe HBT cells is attributed to this transient mechanism. Fully-coupled mixed-mode 3D TCAD simulation of CML SiGe HBT flip-flops verified this sensitivty by isolating the ion-induced shunt current and the substrate-subcolletor funnel current as the dominating upset mechanisms of SiGe HBT flip-flop cells [68]. The impact of scaling of SiGe HBTs with respect to ion-induced transient currents was also investigated, illustrating the expected improvement of SEE mitigation with advanced SiGe HBT technology nodes.

- The impact of deep trench isolation on the single event sensitivity of SiGe HBTs [82]. This study highlighted the important role deep trench isolation plays in confining the sensitive volume of the HBT in bulk platforms for ion strikes by eliminating the lateral depletion that forms with junction isolation. This study also uncovered the increase in the subcollector-substrate funnel current as a result of the confinement of free carriers within the boundaries of the DTI, which impedes ambipolar diffusion away from the subcollector-substrate depletion region. A reduction in the depth of the DTI gives an optimal response of the SiGe HBT for active-area ion strikes, with mimimum enhancements to external-area ion-strikes (assuming that the lateral depletion region does not form).

- The efficacy of N-Ring SiGe HBTs for mitigation of charge-collection and SEU susceptibility [81, 70]. The primary contribution of this work was to re-analyze an experimental SiGe HBT device topology in the context of SEE, using an updated experimental technique, to demonstrate and explain to N-Ring's ineffectiveness at mitigating SEU events in digital circuits. This work illustrates the difficulty in working with radiation data and the care that must be taken in properly designing an experiment and interpreting the results.

- A new cascoded SiGe HBT device for single event mitigation [83, 100, 101]. The greatest contribution of this work was to experimentally validate, through both stand-alone device and digital circuits, the effective mitigation of radiation-induced transient currents and subsequent error events for the in-house developed inverse-mode cascode SiGe HBT. This patented structure is the first of its breed to be introduced to the radiation-effects community, and has demonstrated potential in improving bit-error rates for orbital applications.

- The application of inverse-mode operation for single event mitigation [4, 80]. The contributions of this study were to present the first experimental evidence of the benefits of inverse-mode operation in the context of radiation effects. Despite the trade-off in performance, operating a SiGe HBT in inverse-mode is found to significantly reduce the duration of the ion-induced transeint shunt in addition to isolating the collector terminal from the subcollector-substrate junction of a bulk platform. This gives the advantage of an SOI-like radiation response in a bulk SiGe BiCMOS technology process without having to bear the cost of an SOI process.

- An analysis of the single event susceptibility of mixed-signal components fabricated with SiGe HBTs [37, 36]. Through a collaborative-effort, the VCO, charge pump, and frequency divider cells of a frequnecy synthesis PLL system were

analyzed in the context of SEE. The main contributions coming from this work include a rigorous mathematical model for transient origination and subsequent system impact developed for VCOs, insight into the susceptibility of SiGe HBT charge pump cells to SEE, and the sensitity of programmable frequency dividers to SEE.

8.1 Future Work

As with any field of research, the insight and answers provided by the research I have presented in this dissertation pose new questions to be answered in the field of radiation effects. The topics of interest and specifc questions raised are described here:

- An experimental analysis of the impact of technology scaling on the ion-induced transient currents of a SiGe HBT. The topic of technology scaling has been explored currently through 3D TCAD simulations; however, the need for experimental support is a key piece to any complete scientifc analysis. As SiGe technology moves into it's 4^{th} and device architectures change in addition to the vertical profiles, it becomes increasingly necessary to re-examine the radiation sensitivty of both devices and circuits. Preliminary results have shown an improvement of radiation performance, for both TID and SEE, as SiGe technology has evolved. This work needs to be formalized with both heavy-ion broadbeam measurements of digital and analog/RF circuits in combination with ion microprobing or pulsed-laser analysis of stand-alone SiGe HBTs.

- Experimental study of inverse-mode circuits in a bulk SiGe HBT technology platform. In the study from Chapter 6, digital shift registers in an inverse-mode architecture showed improvements in the error cross-section when irradiated with heavy-ions. To extend this learning to inverse-mode SiGe HBTs in a bulk technology, it is optimal to repeat the heavy-ion broadbeam measurements for bulk inverse-mode circuits. This task was complicated in the initial study by the

lack of industry-supported inverse-mode calibrated compact models, which adds significant complexity to the design process. With appropriate measurements on stand-alone padded SiGe HBT test structures, custom-built inverse-mode paramters can be extracted and integrated with the compact model supplied by an industry partner. This process will allow bulk inverse-mode shift registers to be designed and tested, to validate the claims of improvement from decoupling the subcollector-subtrate terminal from the output.

- Optimization of the vertical germanium profile for inverse-mode operation of SiGe HBTs. In Chapters 5 and 6 it was discussed how the nominal SiGe HBT is tailored from forward-mode operation with respect to the germanium gradient in the base of the transistor. The germanium profile can be tailored for inverse-mode operation; however, which could result in a recovery of loss performance that will narrow window of performance difference between the two modes of operation. Although 3D TCAD simulations have reported that the ion-induced transient current profiles are independent of the germanium profile, this claim must be tested experimentally to verify its credability.

- Fully-coupled mixed-mode 3D TCAD simulations for circuit-level radiation-hadening by design methodologies. Presently an investigation of device-level radiation hardening methodologies has been performed. This works has uncovered the fundamental limitations in mitigating ion-induced transient currents arising from the inherent vertical stack of the SiGe HBT. Although some methodologies have proven to be successfull in adding some level of mitigation (inverse-mode operation), a true radiation-hardened design will be a marriage between device-level hardening techniques and circuit-level mitigation strategies. Fully-coupled mixed-mode 3D TCAD simulations will play a pivotal role in the development of these techniques.

- Full system-level characterization of frequency synthesizer PLLs. To date only individual subcomponents of the frequency synthesis PLL system have been analyzed in the context of SEE. Although the results of these experimental studies have been extended to predict system-level response, closed-loop measurements of the PLL system are necessary to complete the learning of the mixed-signal SEE response. A proposed QPSK testbench, with the PLL actings as the local oscillator has been proposed as a potential candidate for performing this system level study. Initial pusled-laser experiments have uncovered some fundamental obstacles with the current test-bench, requiring a reanalysis of the measurement set-up. Developing design-relevant SEE, FoM for frequency synthesizer PLLs (such as a bit-error rate) will prove to be invaluable to system designers.

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VITA

Stanley D. Phillips was born in Orangeburg, SC in 1984. He received the B.S. degree in electrical engineering in 2006 from the Georgia Institute of Technology. In 2006, Stan joined Dr. John D. Cressler's SiGe research team at the Georgia Institute of Technology. At Georgia Tech, he earned the M.S. degree in electrical and computer engineering in 2009, where his M.S. thesis addressed the development of radiation hardening by process methodologies for improving the single event effect susceptibility of SiGe BiCMOS platforms.

As a continuing Ph.D. student in Dr. Cressler's team, Stan was awarded the Nuclear and Plasma Sciences Society's Phelps Grant in 2011. This grant recognizes graduate students exhibiting "exceptional promise" in NPSS fields who have a track record of "exceptionlly good work." His Ph.D. research focused on characterizing the origination of ion-induced transient currents in SiGe HBTs and the development of subsequent radiation hardening methodologies, on both the deivce and circuit-level. Stan's work has also extended outside the domain of SiGe, touching upon the topic of radiation-effects in other highly-scaled platforms, inclulding silicon-carbide and sub-100 nm CMOS. In 2011, he interned with the Bipolar SPICE Modeling Group at National Semiconductor in Santa Clara, CA. Following the completion of his Ph.D., he will begin employment as a Semiconductor Fab Process Engineer at Texas Instruments in Santa Clara, CA.